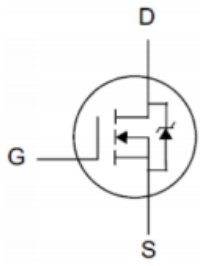
XTMT04N36L

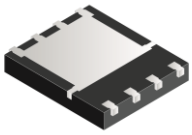
40V N-Channel MOSFET

Product Description

BV_{DSS}	40	V
I_D	36	A
$R_{DS(ON),Typ.}$	7	mΩ

封装 **Package**





PDFN 5×6

General Features

- Enhancement mode
- $R_{DS(ON),typ.}$=7 mΩ@V_{GS}=10V
- Fast Switching
- High efficiency

Applications

- Synchronous Rectification
- UPS Inverter

Device	Package	Marking
XTMT04N36L	PDFN5x6	XTMT04N36L

Absolute Maximum Ratings T_j=25℃

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	40	V
V_{GSS}	Gate-to-Source Voltage	±20	
I_D	Continuous Drain Current	36	A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	144	
E_{AS}	Single Pulse Avalanche Energy	64	mJ
P_D	Power Dissipation	34	W
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.1	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	℃/W

Electrical Characteristics T_j=25℃

OFF Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
BV_{DSS}	Drain-to-Source Breakdown Voltage	40	-	-	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	-	-	1	uA	V_{DS}=40V, V_{GS}=0V
		-	-	100		V_{DS}=32V, V_{GS}=0V, T_J=125℃
I_{GSS}	Gate-to-Source Leakage Current	-	-	+100	nA	V_{GS}=+20V, V_{DS}=0V
		-	-	-100		V_{GS}=-20V, V_{DS}=0V

ON Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	-	7	9	mΩ	V_{GS}=10V, I_D=20A
		-	10	13	mΩ	V_{GS}=4.5V, I_D=10A
$V_{GS(TH)}$	Gate Threshold Voltage	1.2	1.7	2.3	V	V_{DS}=V_{GS}, I_D=250uA
Rg	Gate Resistance		2.1		Ω	f=1.0MHz

Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
C_{iss}	Input Capacitance	-	870	-	pF	V_{GS}=0V, V_{DS}=20V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	-	15	-		
C_{oss}	Output Capacitance	-	250	-		
Q_g	Total Gate Charge	-	14	-	nC	V_{DD}=20V, I_D=20A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	-	3	-		
Q_{gd}	Gate-to-Drain (Miller) Charge	-	2	-		

Resistive Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$t_{d(ON)}$	Turn-on Delay Time	-	5.8	-	ns	V_{DD}=20V, I_D=20A, V_{GS}=10V Rg=3Ω
t_{rise}	Rise Time	-	43	-		
$t_{d(OFF)}$	Turn-Off Delay Time	-	15	-		
t_{fall}	Fall Time	-	4.5	-		

Source-Drain Body Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{SD}	Continuous Source Current[1]	-	-	36	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[1]	-	-	144		
V_{SD}	Diode Forward Voltage	-	-	1.2	V	I_S=20A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	-	17	-	ns	I_F=20A, di_F/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	-	6.2	-	uC	

[1] Pulse width≤380μs; duty cycle≤2%

Typical Characteristics

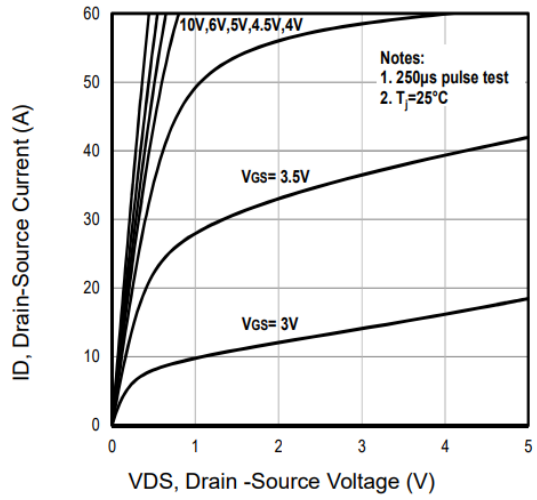


Fig1. Typical Output Characteristics

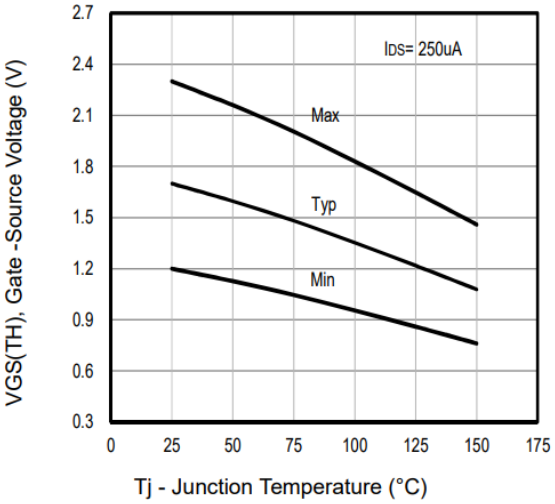


Fig2. Typical $V_{GS(TH)}$ Gate -Source Voltage Vs. Tj

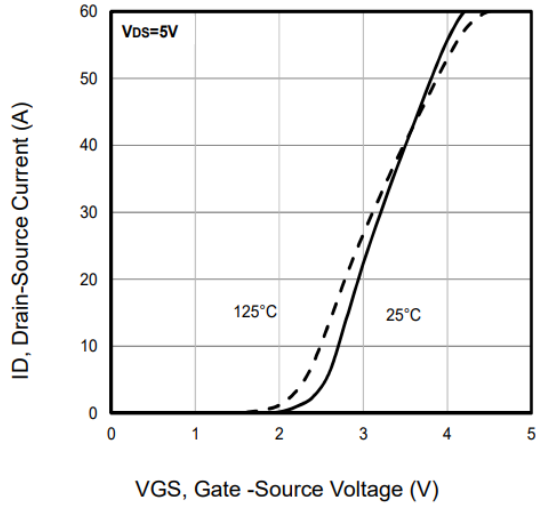


Fig3. Typical Transfer Characteristics

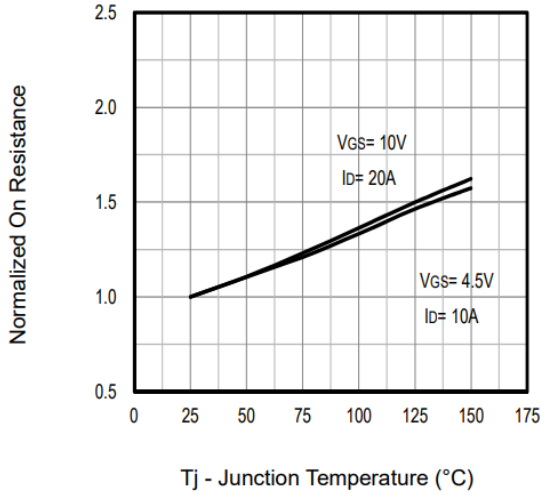


Fig4. Typical Normalized On-Resistance Vs. Tj

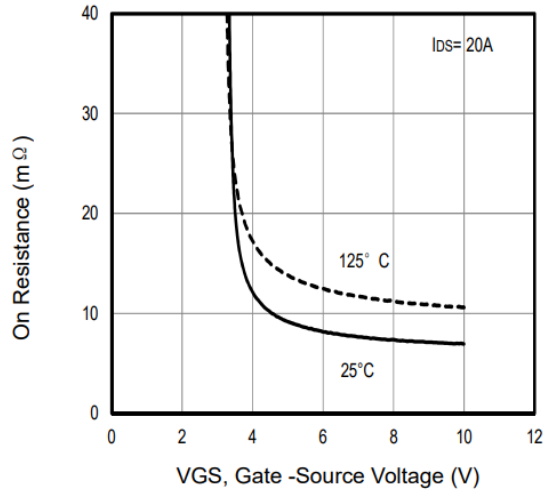


Fig5. Typical On Resistance Vs Gate -Source Voltage

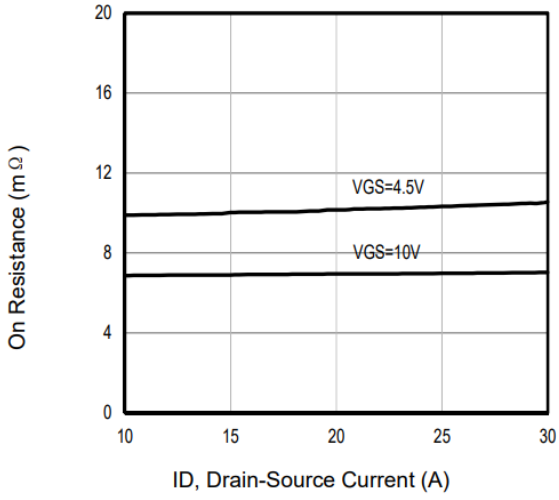


Fig6. Typical On Resistance Vs Drain Current

Typical Characteristics

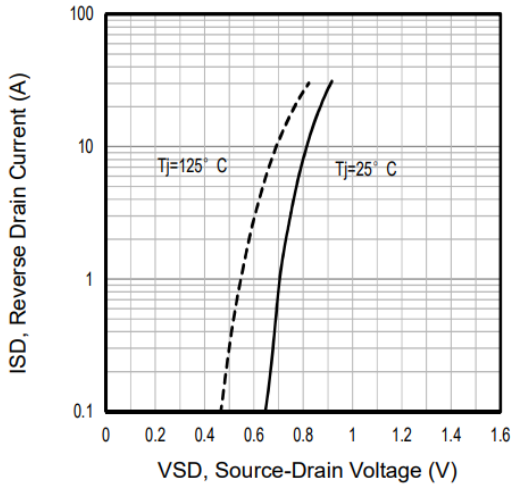


Fig7. Typical Source-Drain Diode Forward Voltage

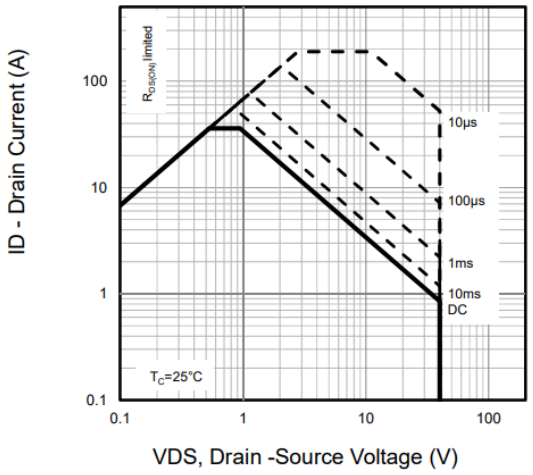


Fig8. Maximum Safe Operating Area

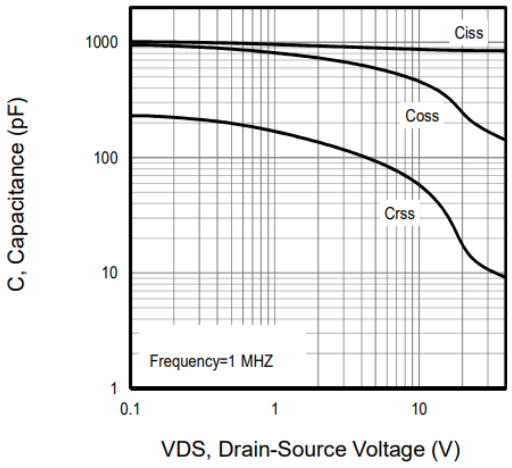


Fig9. Typical Capacitance Vs. Drain-Source Voltage

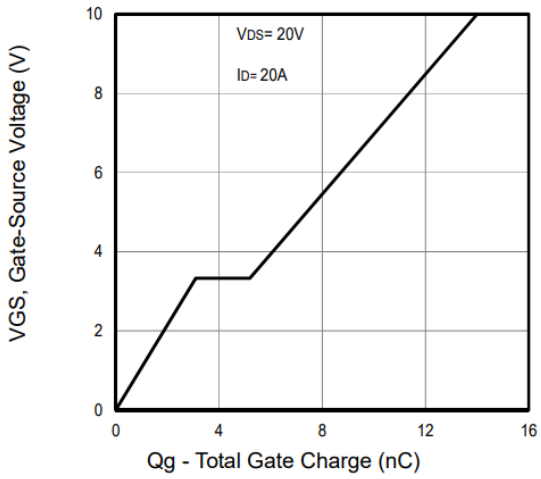


Fig10. Typical Gate Charge Vs. Gate-Source Voltage

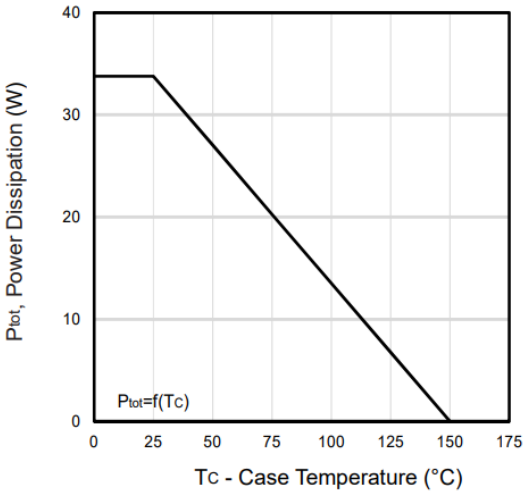


Fig11. Power Dissipation Vs. Case Temperature

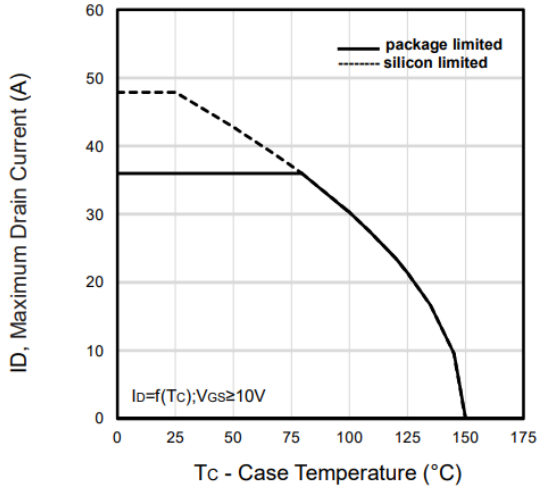


Fig12. Maximum Drain Current Vs. Case Temperature

Test Circuits and Waveforms

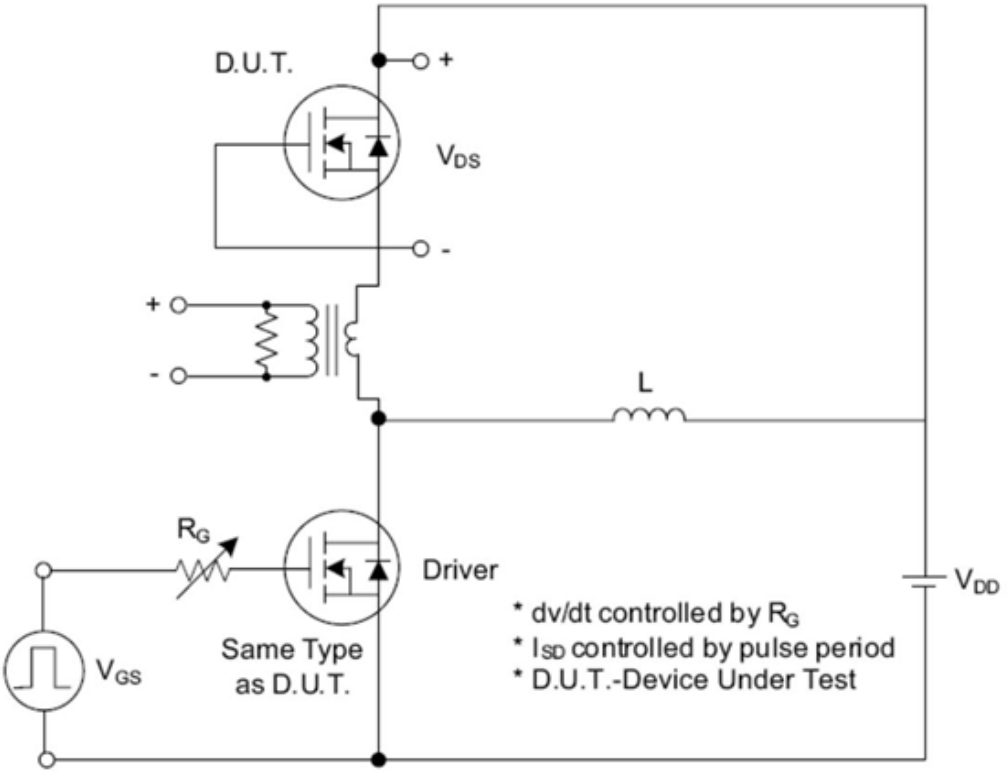


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

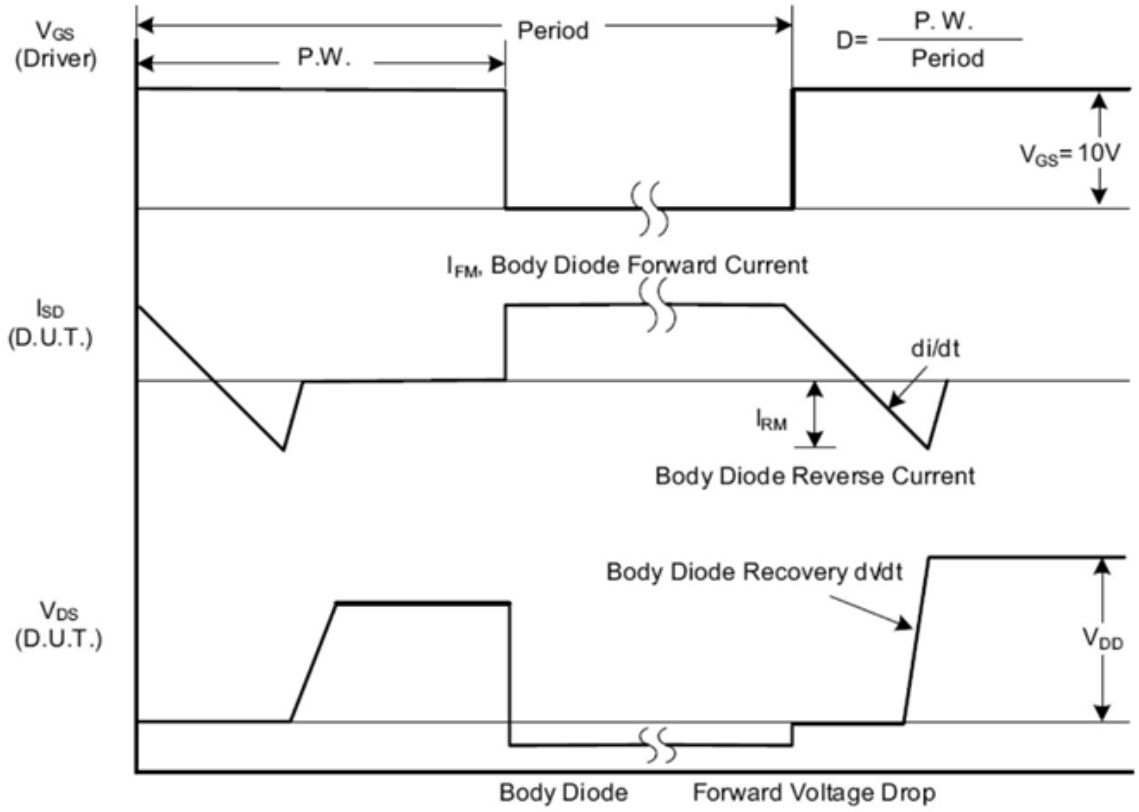


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

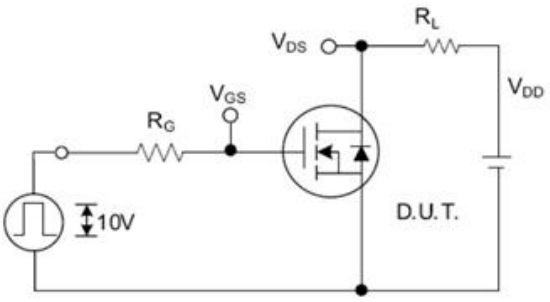


Fig. 2.1 Switching Test Circuit

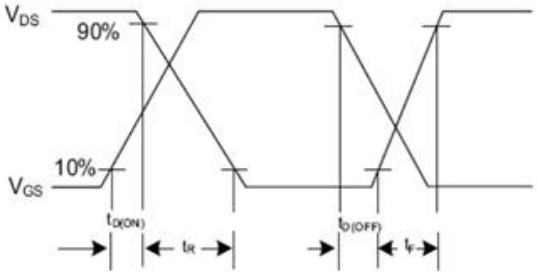


Fig. 2.2 Switching Waveforms

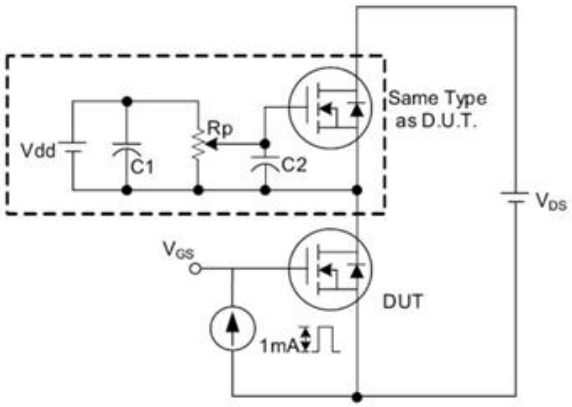


Fig. 3 . 1 Gate Charge Test Circuit

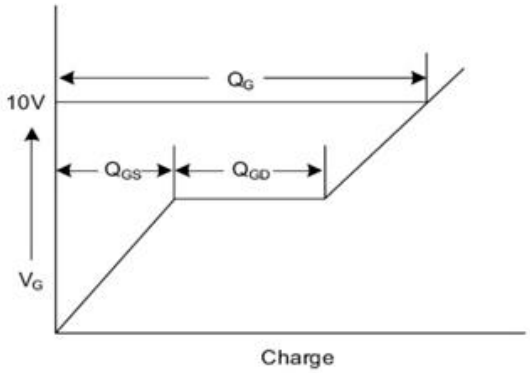


Fig. 3 . 2 Gate Charge Waveform

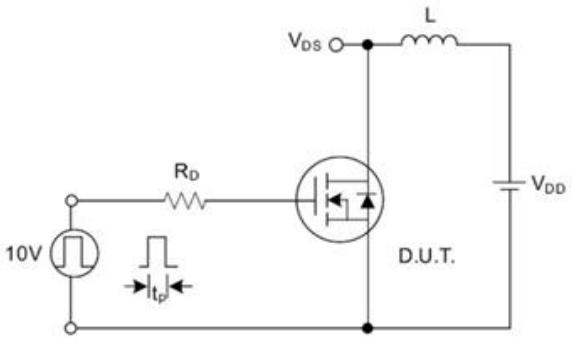


Fig. 4.1 Unclamped Inductive Switching Test Circuit

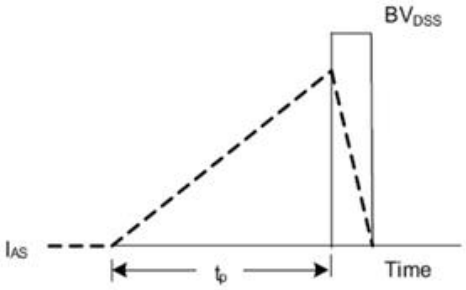


Fig. 4.2 Unclamped Inductive Switching Waveforms