



XTMT15N50F1

150V N-Channel MOSFET

Product Description

BV_{DSS}	150	V
I_D	50	A
$R_{DS(ON),Typ.}$	0.03	Ω

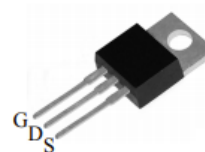
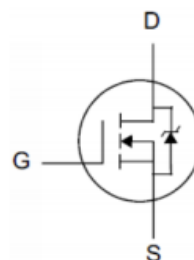
General Features

- Proprietary New Planar Technology
- $R_{DS(ON),typ.}=30\text{ m}\Omega@V_{GS}=10V$
- Fast Recovery Body Diode
- Low Gate Charge Minimize Switching Loss

Applications

- Uninterruptible Power Supply
- Power Switching application

封装 Package



TO-220

Device	Package	Marking
XTMT15N50F1	TO-220	XTMT15N50F1

Absolute Maximum Ratings $T_j=25^\circ\text{C}$

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	150	V
V_{GSS}	Gate-to-Source Voltage	± 20	
I_D	Continuous Drain Current	50	A
I_{DM}	Pulsed Drain Current at $V_{GS}=10V$	180	
E_{AS}	Single Pulse Avalanche Energy	295	mJ
P_D	Power Dissipation	151	W
	Derating Factor above 25°C	1.20	W/ $^\circ\text{C}$
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	$^\circ\text{C}$
$T_J \& T_{STG}$	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.



Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.83	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	$^{\circ}C/W$

Electrical Characteristics $T_j=25^{\circ}C$

OFF Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
BV_{DSS}	Drain-to-Source Breakdown Voltage	150	-	-	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	-	-	1	uA	$V_{DS}=150V, V_{GS}=0V$
		-	-	100		$V_{DS}=120V, V_{GS}=0V, T_J=125^{\circ}C$
I_{GSS}	Gate-to-Source Leakage Current	-	-	+100	nA	$V_{GS}=+20V, V_{DS}=0V$
		-	-	-100		$V_{GS}=-20V, V_{DS}=0V$

ON Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	-	30	38	m Ω	$V_{GS}=10V, I_D=30A$
$V_{GS(TH)}$	Gate Threshold Voltage	3.0	3.7	4.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$

**Dynamic Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
C_{iss}	Input Capacitance	-	2447	-	pF	$V_{GS}=0V$, $V_{DS}=25V$, $f=1.0MHz$
C_{rss}	Reverse Transfer Capacitance	-	41	-		
C_{oss}	Output Capacitance	-	153	-		
R_G	Gate Series Resistance		2.5		Ω	$f=1.0MHz$
Q_g	Total Gate Charge	-	56	-	nC	$V_{DD}=100V$, $I_D=30A$, $V_{GS}=0$ to 10V
Q_{gs}	Gate-to-Source Charge	-	12	-		
Q_{gd}	Gate-to-Drain (Miller) Charge	-	18	-		

Resistive Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$t_{d(ON)}$	Turn-on Delay Time	-	28	-	ns	$V_{DD}=100V$, $I_D=30A$, $V_{GS}=10V$ $R_g=2.5\Omega$
t_{rise}	Rise Time	-	30	-		
$t_{d(OFF)}$	Turn-Off Delay Time	-	95	-		
t_{fall}	Fall Time	-	40	-		

Source-Drain Body Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{SD}	Continuous Source Current ^[1]	-	-	50	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current ^[1]	-	-	180		
V_{SD}	Diode Forward Voltage	-	0.85	1.3	V	$I_S=30A$, $V_{GS}=0V$
t_{rr}	Reverse Recovery Time	-	48	-	ns	$I_F=30A$, $di_F/dt=100A/\mu s$
Q_{rr}	Reverse Recovery Charge	-	78	-	μC	

[1] Pulse width $\leq 380\mu s$; duty cycle $\leq 2\%$



Typical Characteristic

Figure 1: Power Dissipation

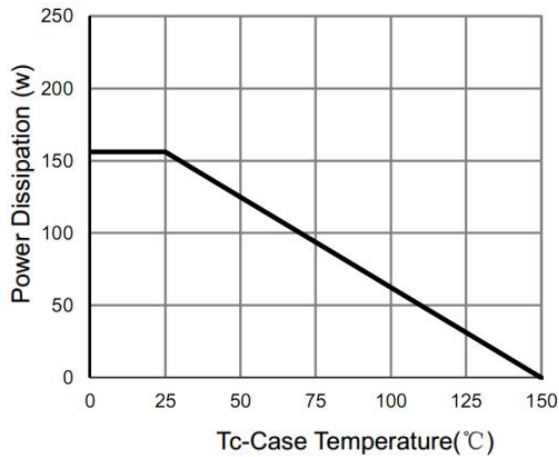


Figure 2: Drain Current

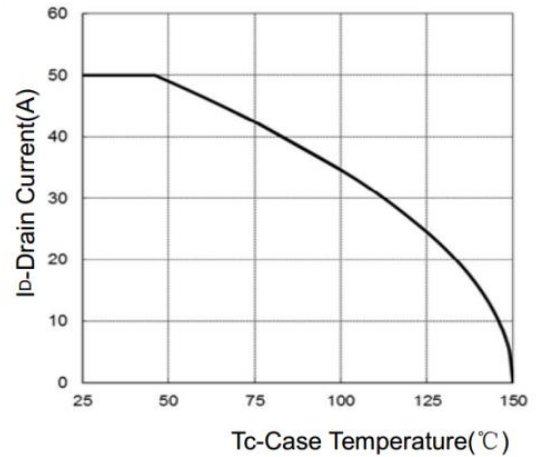


Figure 3: Safe Operation Area

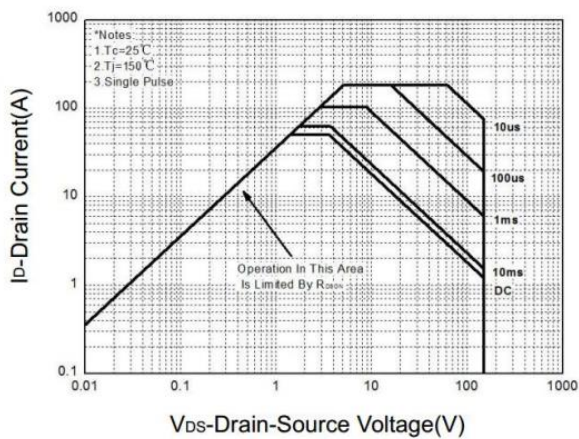


Figure 4: Thermal Transient Impedance

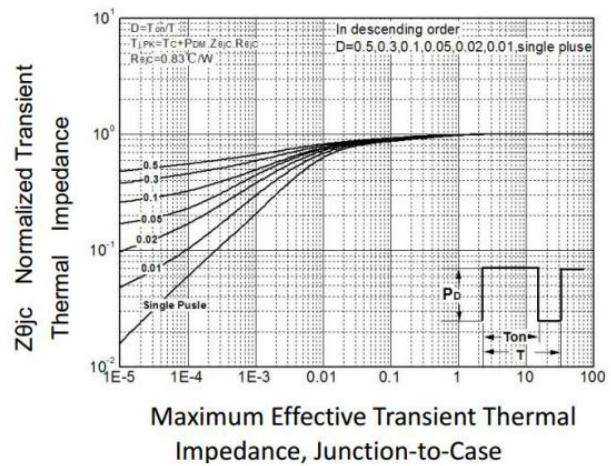


Figure 5: Output Characteristics

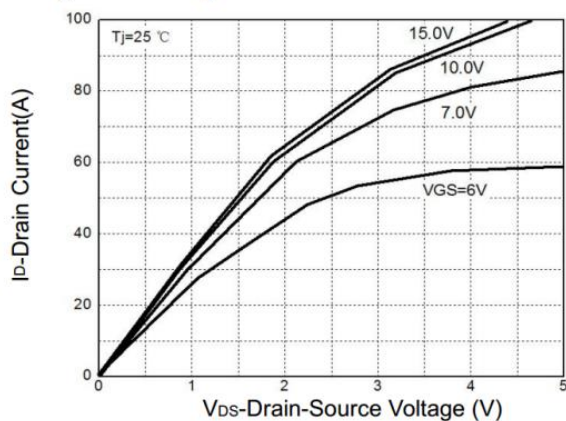
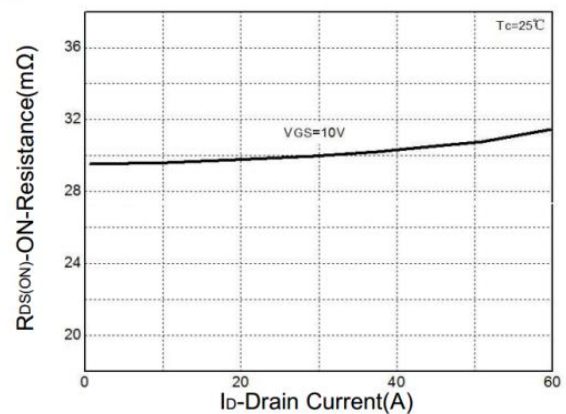


Figure 6: Drain-Source On Resistance





Typical Characteristics(Cont.)

Figure 7: On-Resistance vs. Temperature

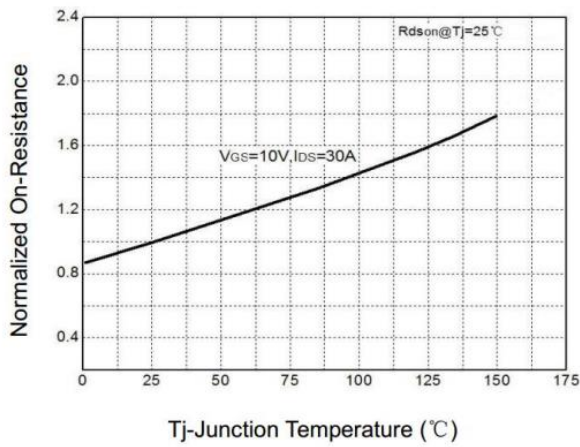


Figure 8: Source-Drain Diode Forward

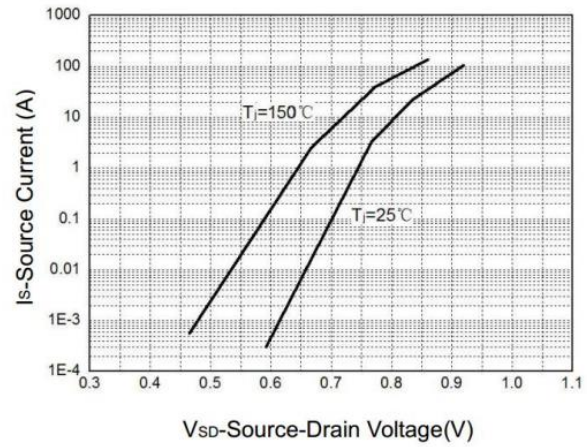


Figure 9: Capacitance Characteristics

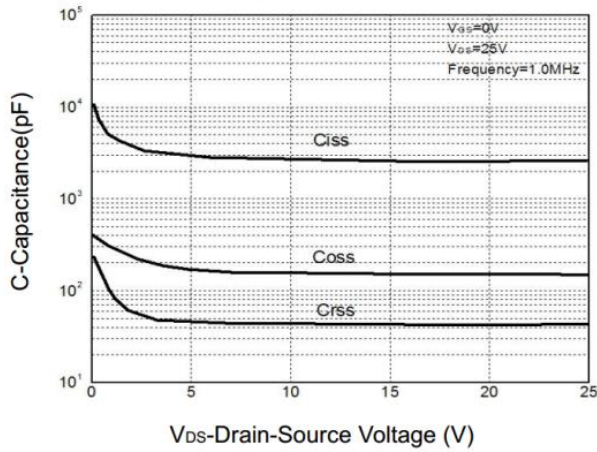
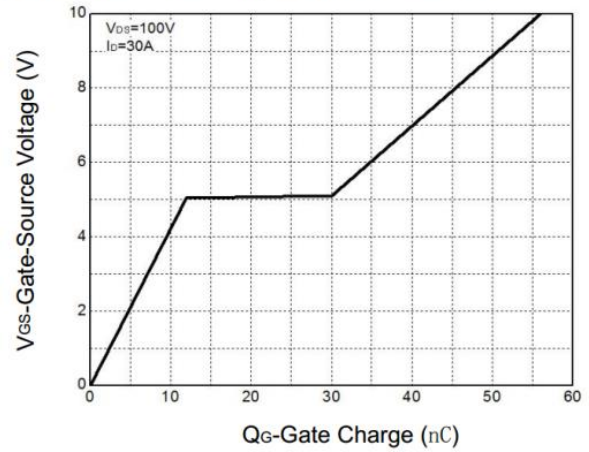


Figure 10: Gate Charge Characteristics





Test Circuits and Waveforms

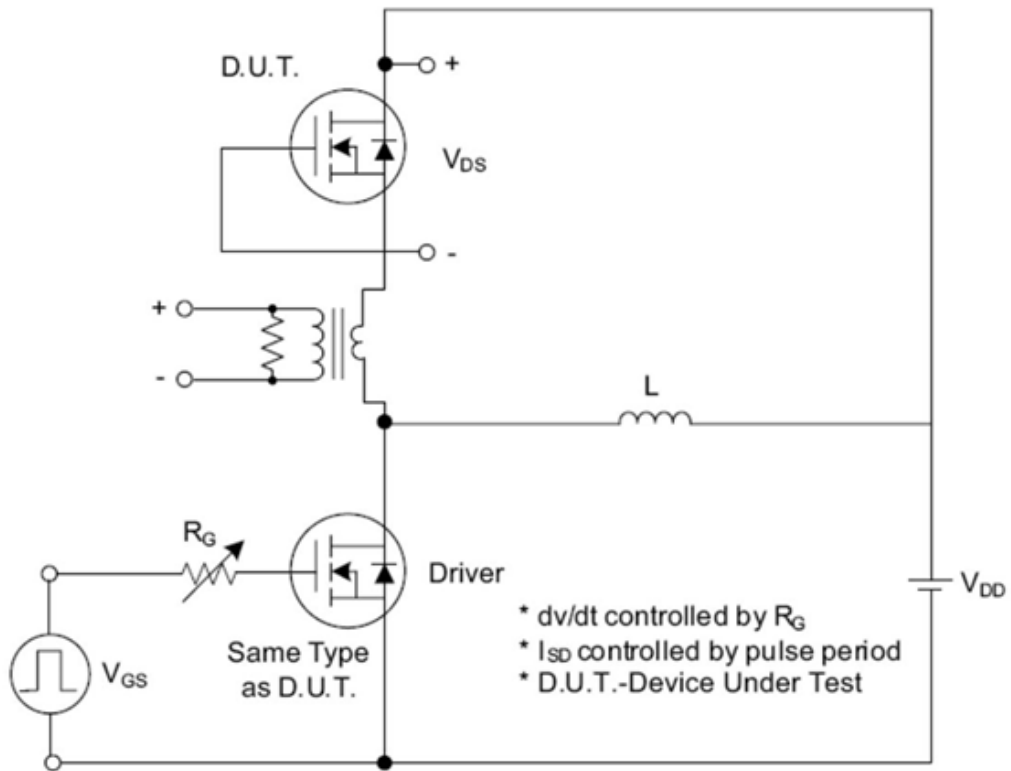


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

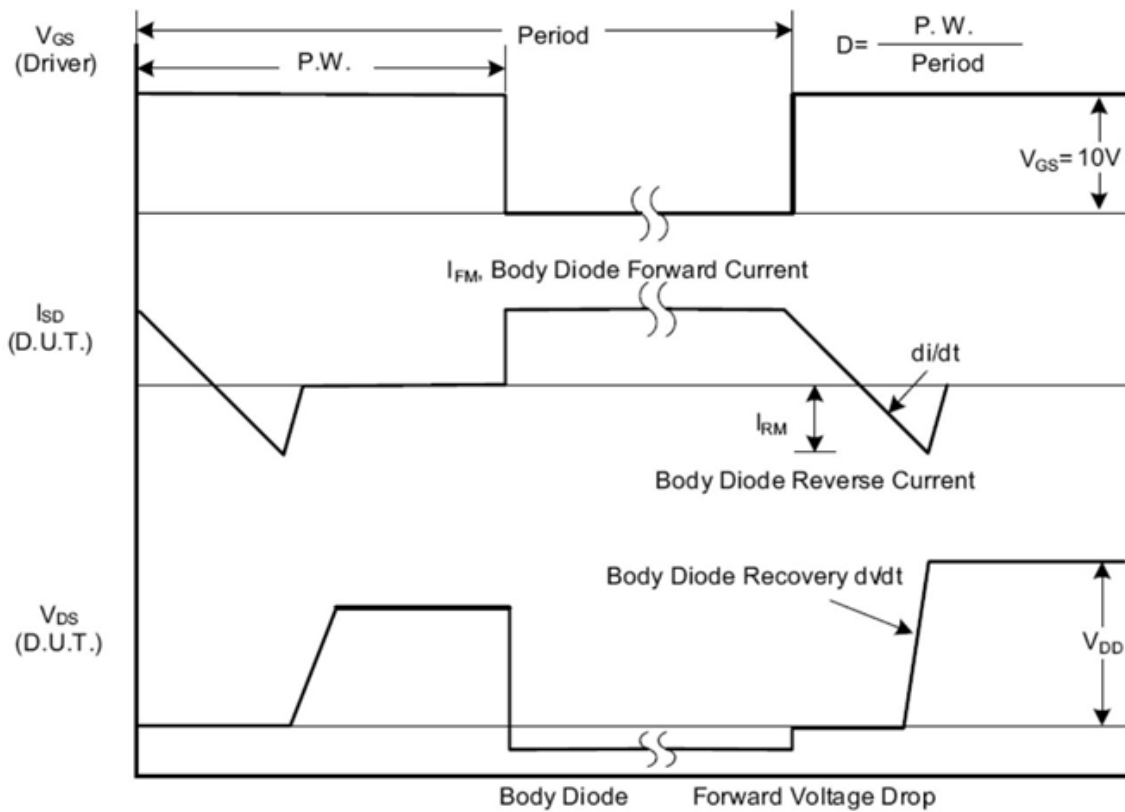


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms



Test Circuits and Waveforms (Cont.)

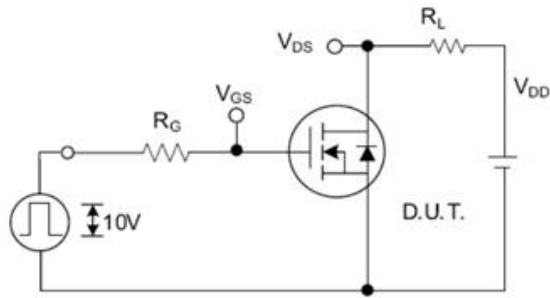


Fig. 2.1 Switching Test Circuit

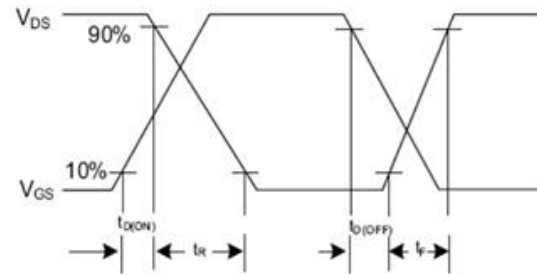


Fig. 2.2 Switching Waveforms

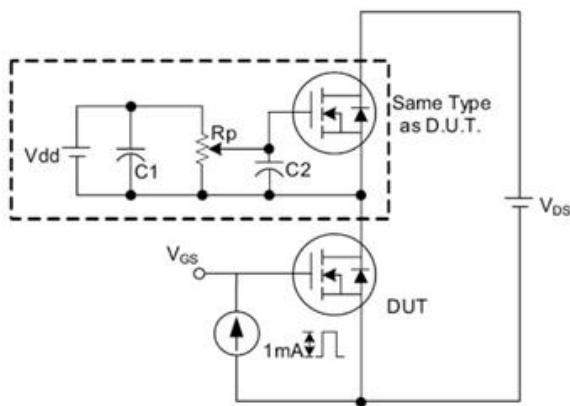


Fig. 3.1 Gate Charge Test Circuit

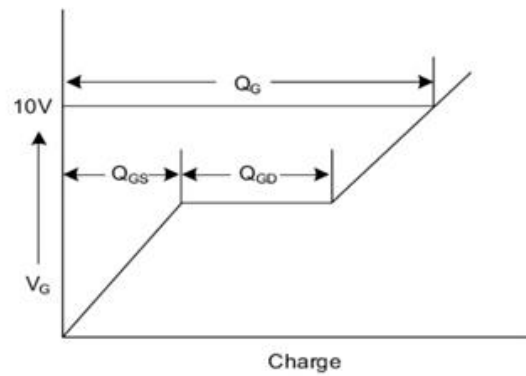


Fig. 3.2 Gate Charge Waveform

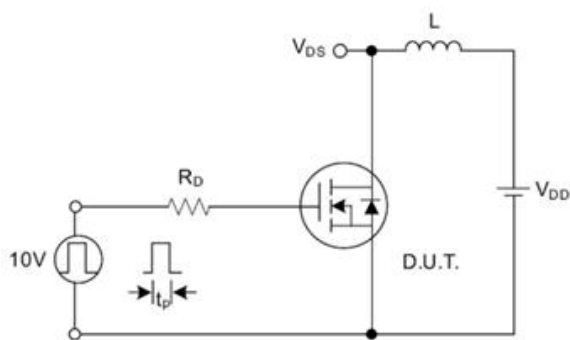


Fig. 4.1 Unclamped Inductive Switching Test Circuit

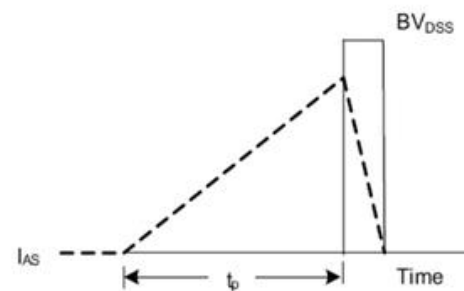


Fig. 4.2 Unclamped Inductive Switching Waveforms