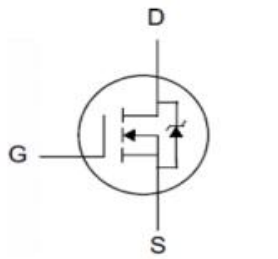
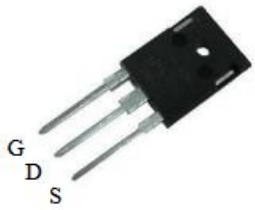
XTMF120N12E

1200V N-Channel MOSFET

封装 **Package**





TO-247

Product Description

BV_{DSS}	1200	V
I_D	12	A
$R_{DS(ON),Typ.}$	1.2	Ω

General Features

- Fast Switching
- $R_{DS(ON),typ.}$=1.2Ω@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Applications

- Adaptor
- Charger
- SMPS Standby Power

Device	Package	Marking
XTMF120N12E	TO-247	XTMF120N12E

Absolute Maximum Ratings T_j=25℃

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	1200	V
V_{GSS}	Gate-to-Source Voltage	±30	
I_D	Continuous Drain Current	12	A
	Continuous Drain Current @ Tc=100℃	7	
I_{DM}	Pulsed Drain Current at V_{GS}=10V	48	
E_{AS}	Single Pulse Avalanche Energy	700	mJ
P_D	Power Dissipation	380	W
	Derating Factor above 25℃	3.04	W/℃
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.329	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	℃/W

Electrical Characteristics T_j=25℃

OFF Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
BV_{DSS}	Drain-to-Source Breakdown Voltage	1200	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	uA	V_{DS}=1200V, V_{GS}=0V
		--	--	250		V_{DS}=960V, V_{GS}=0V, T_J=125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	1.2	1.4	Ω	V_{GS}=10V, I_D=6A
$V_{GS(TH)}$	Gate Threshold Voltage	2.5	--	4.5	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance	--	15	--	S	V_{DS}=15V,I_D=6A

Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
C_{iss}	Input Capacitance	--	3300	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	50	--		
C_{oss}	Output Capacitance	--	300	--		
Q_g	Total Gate Charge	--	80	--	nC	V_{DD}=600V, I_D=6A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	18	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	38	--		

Resistive Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$td_{(ON)}$	Turn-on Delay Time	-	15	-	nS	VDD=600V, ID=6A, VGS=15V RG=4.7Ω
t_{rise}	Rise Time	-	10	-		
$td_{(OFF)}$	Turn-Off Delay Time	-	50	-		
t_{fall}	Fall Time	-	33	-		

Source-Drain Body Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{SD}	Continuous Source Current[1]	--	--	12	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current[1]	--	--	48		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=12A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	1400	--	ns	V_{GS}=0V I_F=12A, di_F/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	18	--	uC	

[1] Pulse width≤380μs; duty cycle≤2%

Typical Characteristics

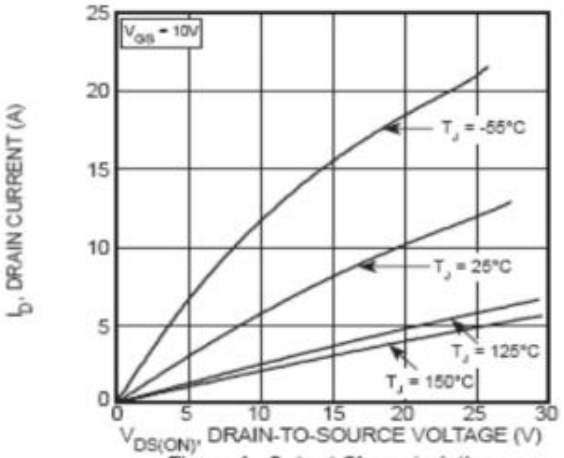


Figure 1, Output Characteristics

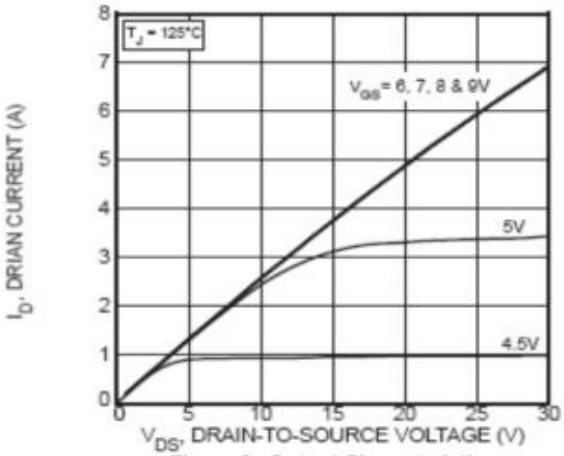


Figure 2, Output Characteristics

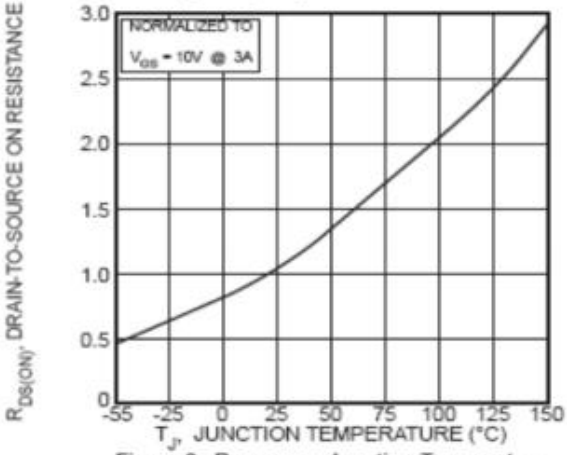


Figure 3, $R_{DS(ON)}$ vs Junction Temperature

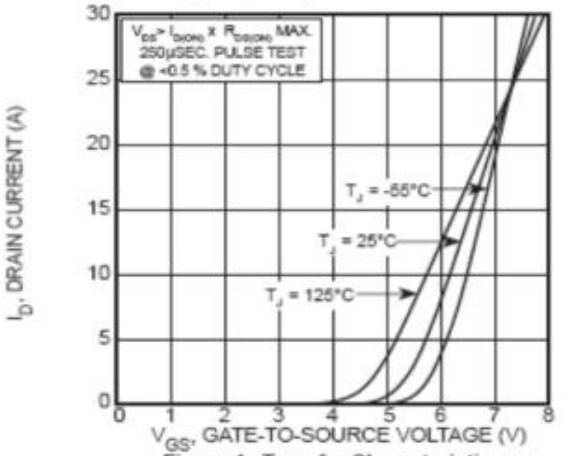


Figure 4, Transfer Characteristics

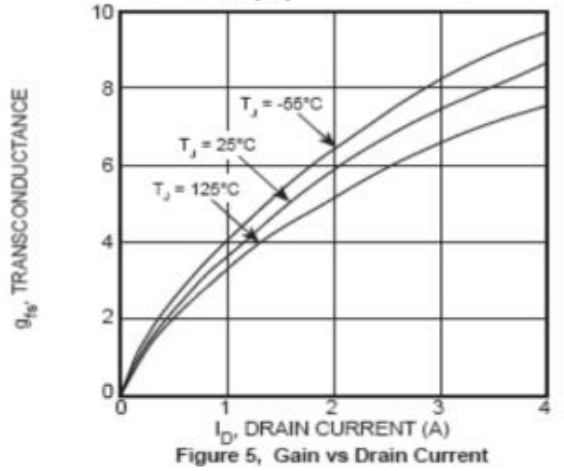


Figure 5, Gain vs Drain Current

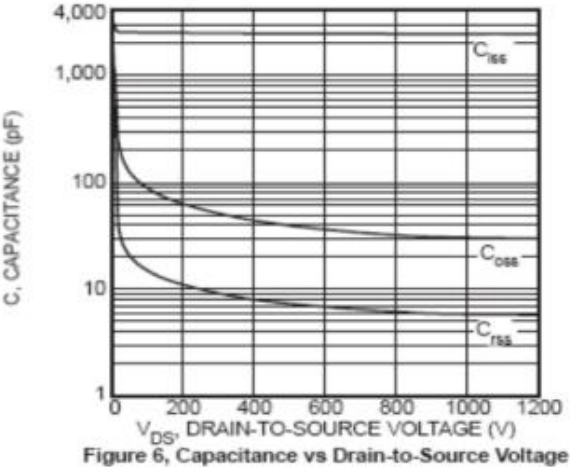


Figure 6, Capacitance vs Drain-to-Source Voltage

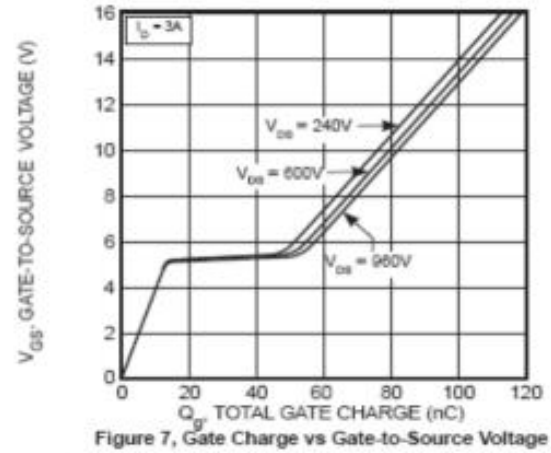


Figure 7, Gate Charge vs Gate-to-Source Voltage

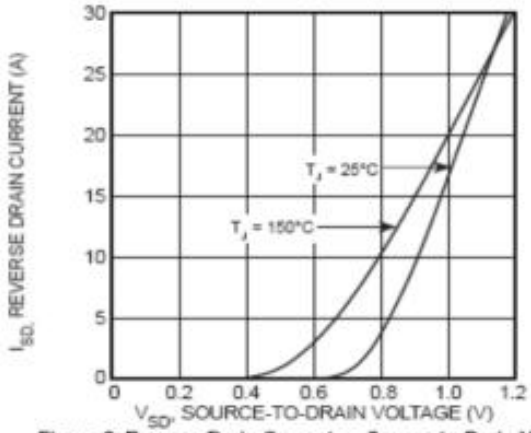


Figure 8, Reverse Drain Current vs Source-to-Drain Voltage

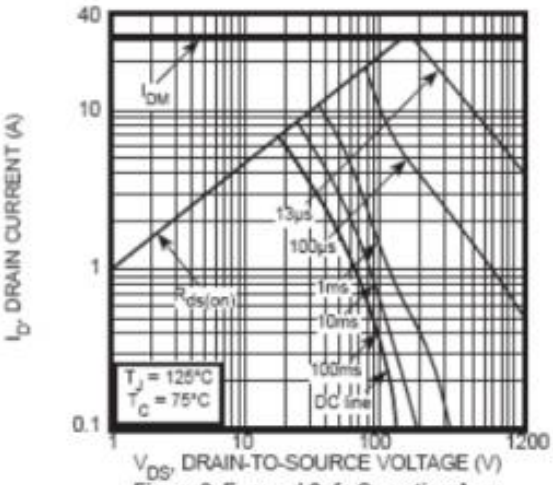


Figure 9, Forward Safe Operating Area

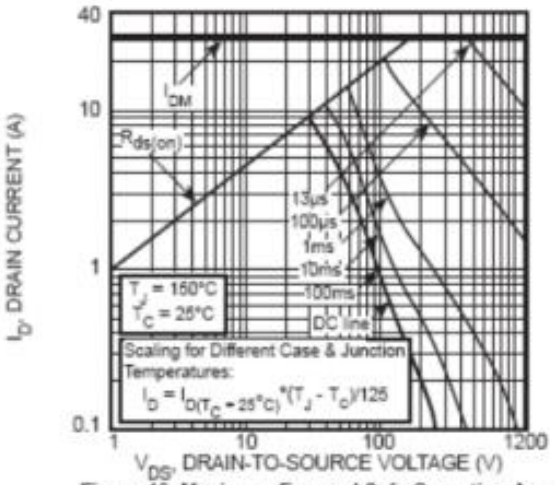


Figure 10, Maximum Forward Safe Operating Area

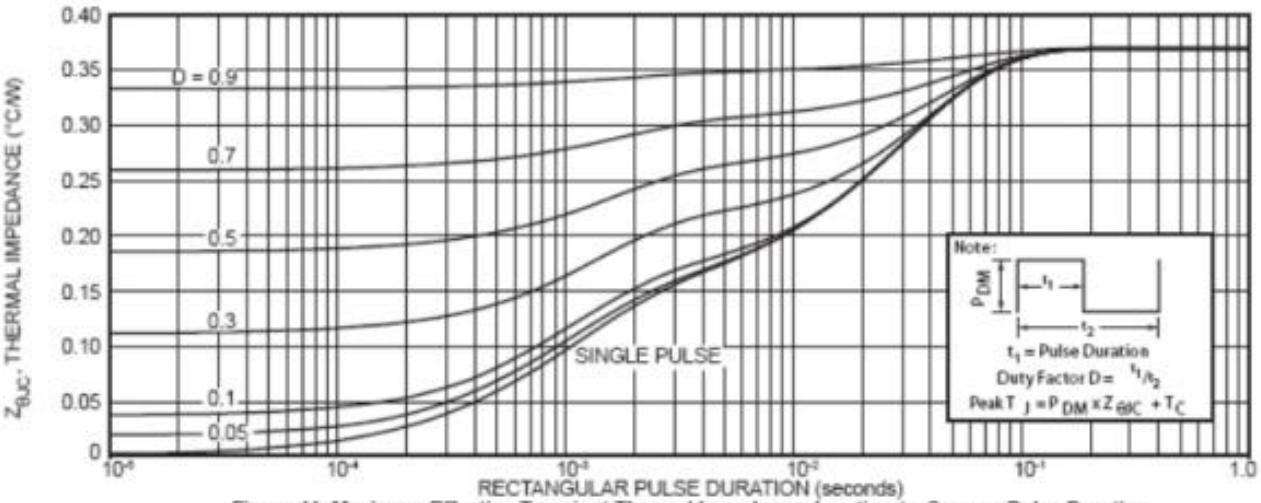


Figure 11. Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

Typical Characteristics(Cont.)

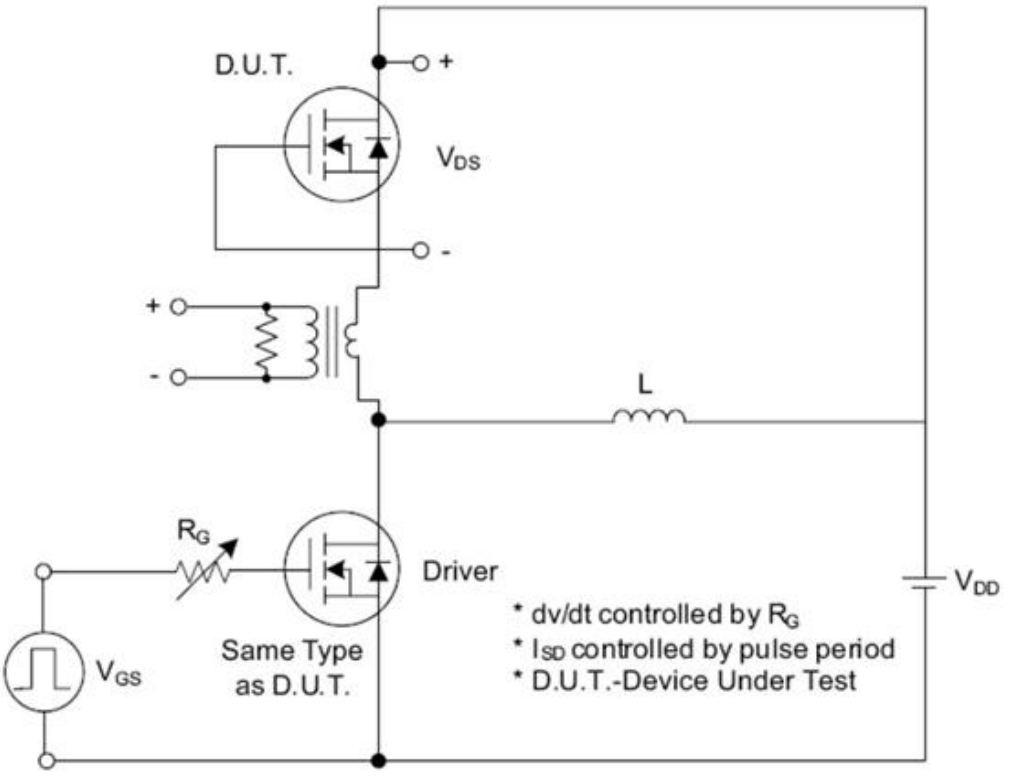


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

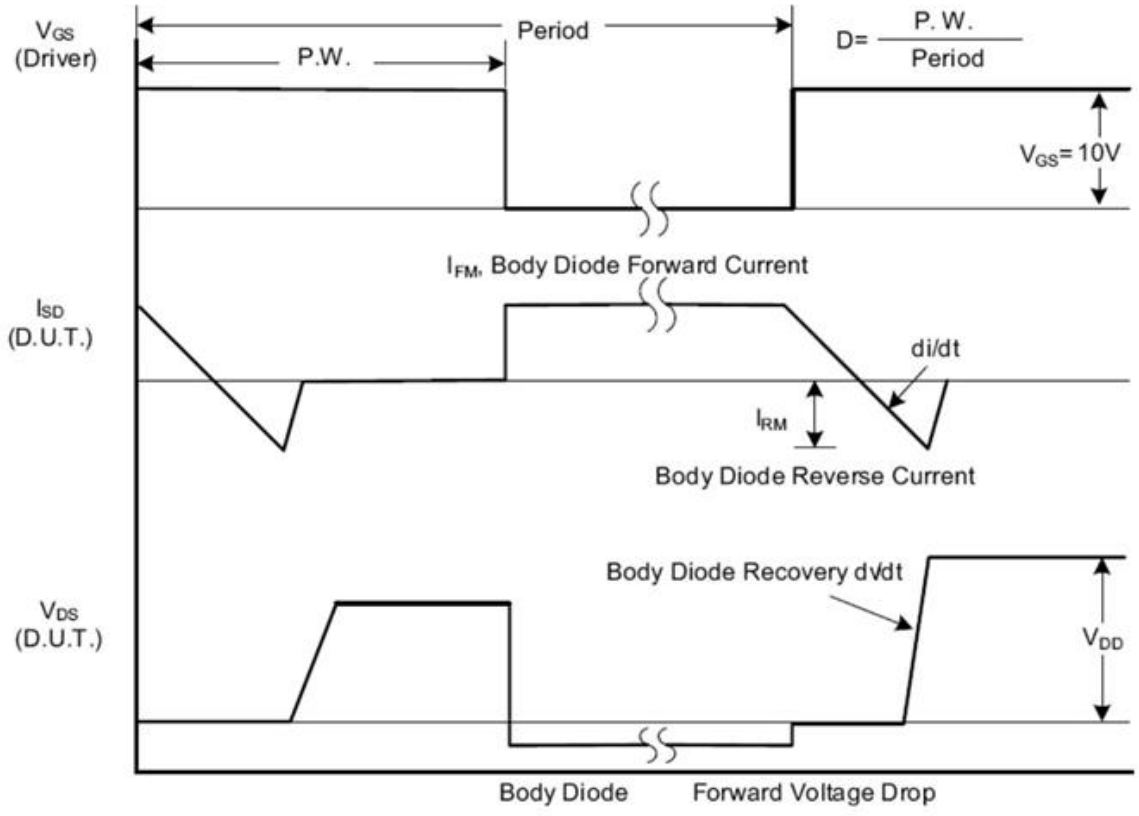


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

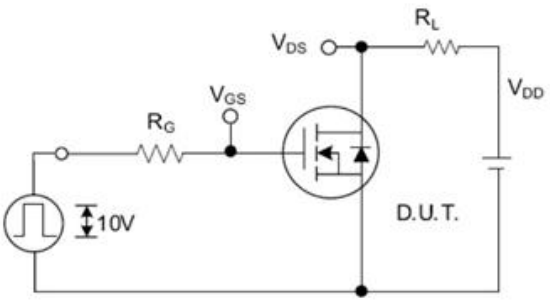


Fig. 2.1 Switching Test Circuit

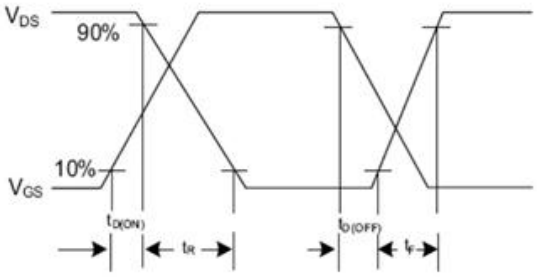


Fig. 2.2 Switching Waveforms

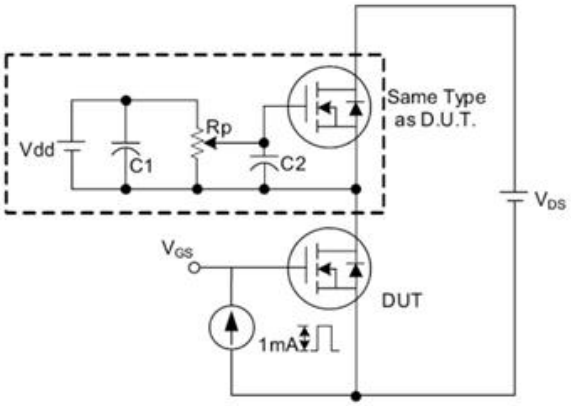


Fig. 3 . 1 Gate Charge Test Circuit

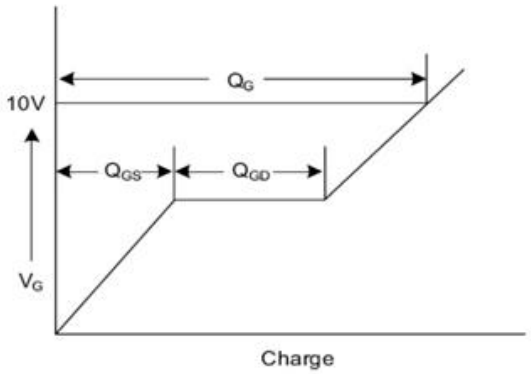


Fig. 3 . 2 Gate Charge Waveform

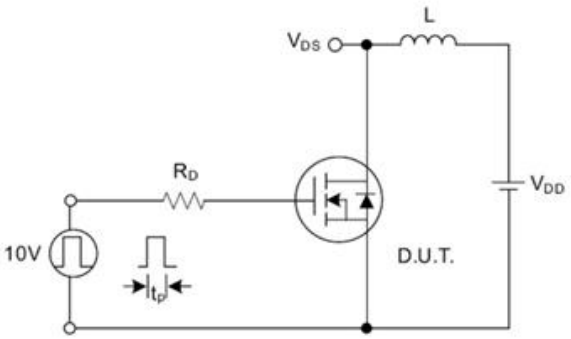


Fig. 4.1 Unclamped Inductive Switching Test Circuit

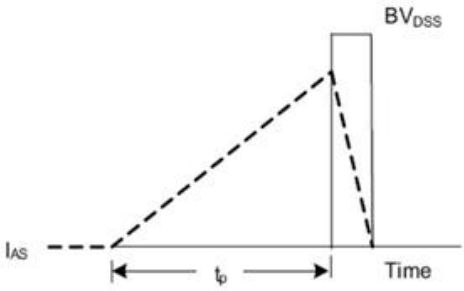


Fig. 4.2 Unclamped Inductive Switching Waveforms