



XTMT15N03N

150V N-Channel MOSFET

Product Description

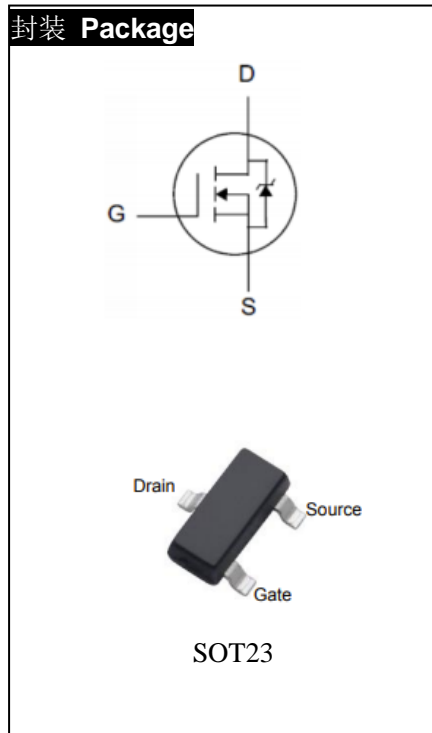
BV_{DSS}	150	V
I_D	3	A
$R_{DS(ON),Typ.}$	0.55	Ω

General Features

- Proprietary New Planar Technology
- $R_{DS(ON),typ.}=550m\Omega@V_{GS}=4.5V$
- Fast Recovery Body Diode
- Low Gate Charge Minimize Switching Loss

Applications

- Synchronous Rectification
- UPS Inverter



Device	Package	Marking
XTMT15N03N	SOT23	XTMT15N03N

Absolute Maximum Ratings $T_j=25^\circ\text{C}$

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-to-Source Voltage	150	V
V_{GSS}	Gate-to-Source Voltage	± 20	
I_D	Continuous Drain Current	3	A
I_{DM}	Pulsed Drain Current at $V_{GS}=10V$	12	
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	$^\circ\text{C}$
$T_J \& T_{STG}$	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

**Electrical Characteristics** $T_j=25^{\circ}\text{C}$ **OFF Characteristics**

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
BV_{DSS}	Drain-to-Source Breakdown Voltage	150	-	-	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	-	-	1	uA	$V_{DS}=150V, V_{GS}=0V$
		-	-	100		$V_{DS}=120V, V_{GS}=0V, T_J=125^{\circ}\text{C}$
I_{GSS}	Gate-to-Source Leakage Current	-	-	+100	nA	$V_{GS}=+20V, V_{DS}=0V$
		-	-	-100		$V_{GS}=-20V, V_{DS}=0V$

ON Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	-	550	635	m Ω	$V_{GS}=4.5V, I_D=1A$
$V_{GS(TH)}$	Gate Threshold Voltage	1.1	-	2.1	V	$V_{DS}=V_{GS}, I_D=250\mu A$

Source-Drain Body Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{SD}	Continuous Source Current ^[1]	-	-	3	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current ^[1]	-	-	12		
V_{SD}	Diode Forward Voltage	-	-	1.2	V	$I_S=1A, V_{GS}=0V$

[1] Pulse width $\leq 380\mu s$; duty cycle $\leq 2\%$



Test Circuits and Waveforms

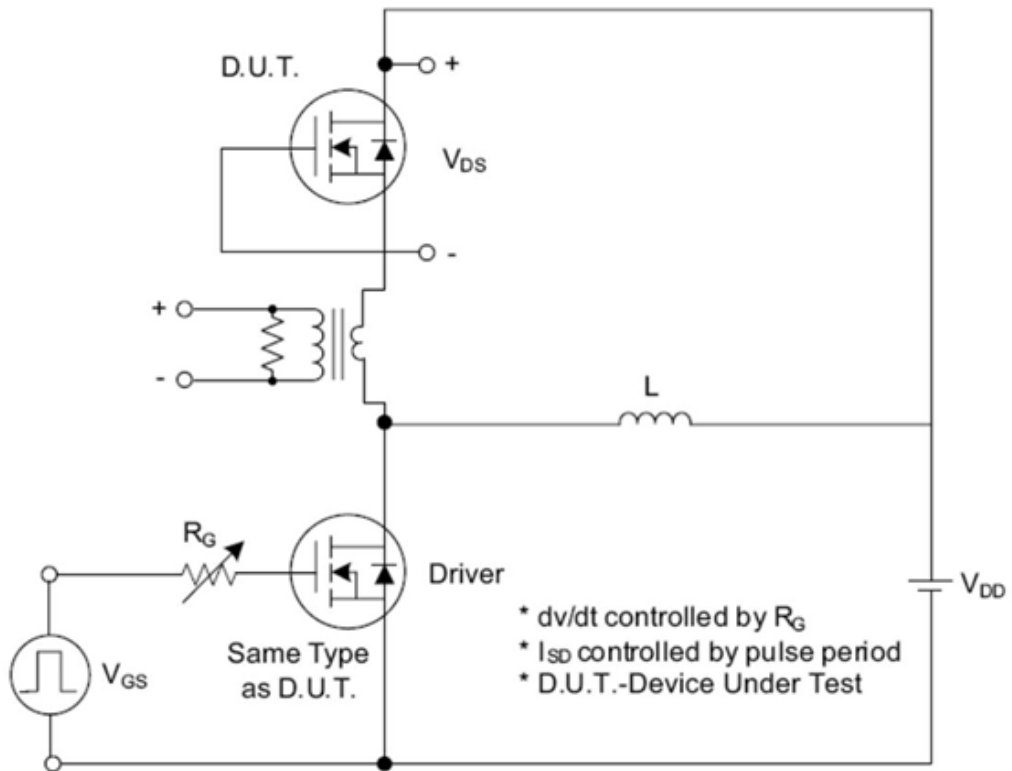


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

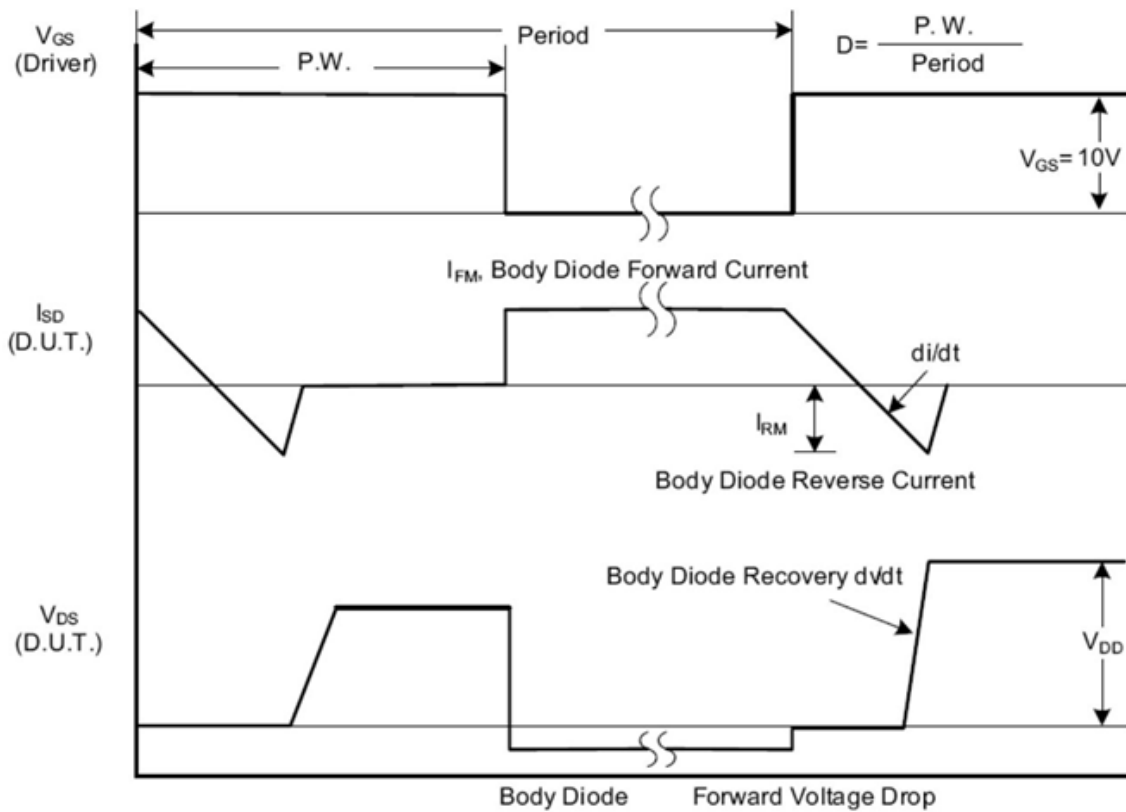


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms



Test Circuits and Waveforms (Cont.)

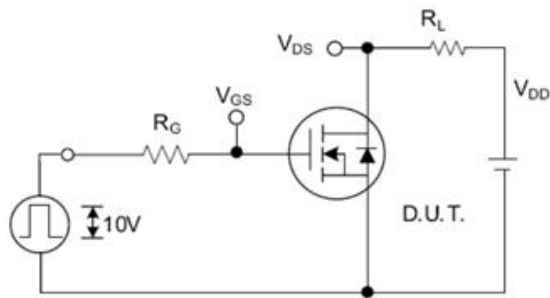


Fig. 2.1 Switching Test Circuit

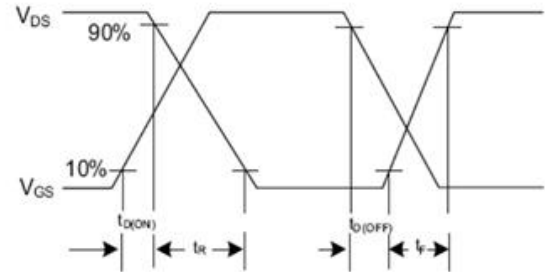


Fig. 2.2 Switching Waveforms

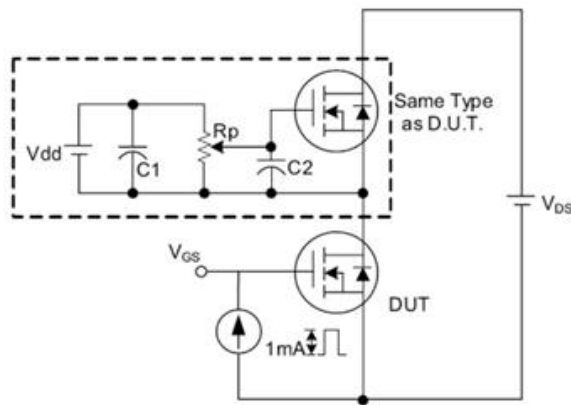


Fig. 3.1 Gate Charge Test Circuit

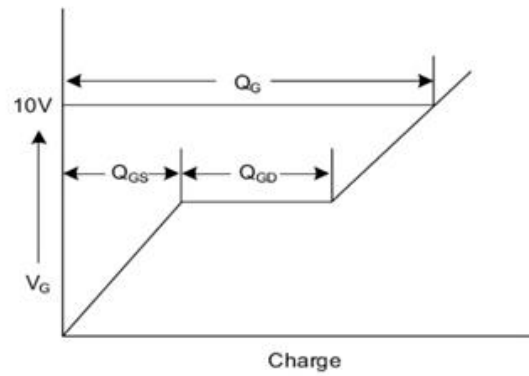


Fig. 3.2 Gate Charge Waveform

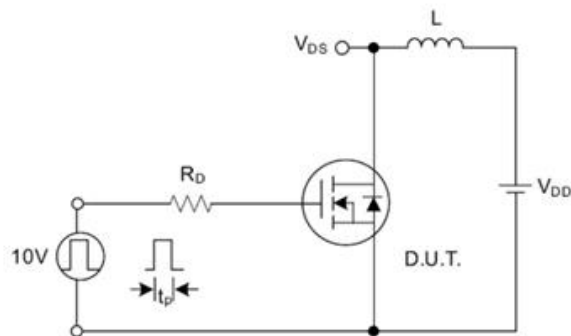


Fig. 4.1 Unclamped Inductive Switching Test Circuit

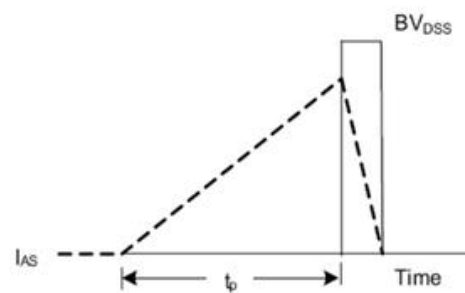
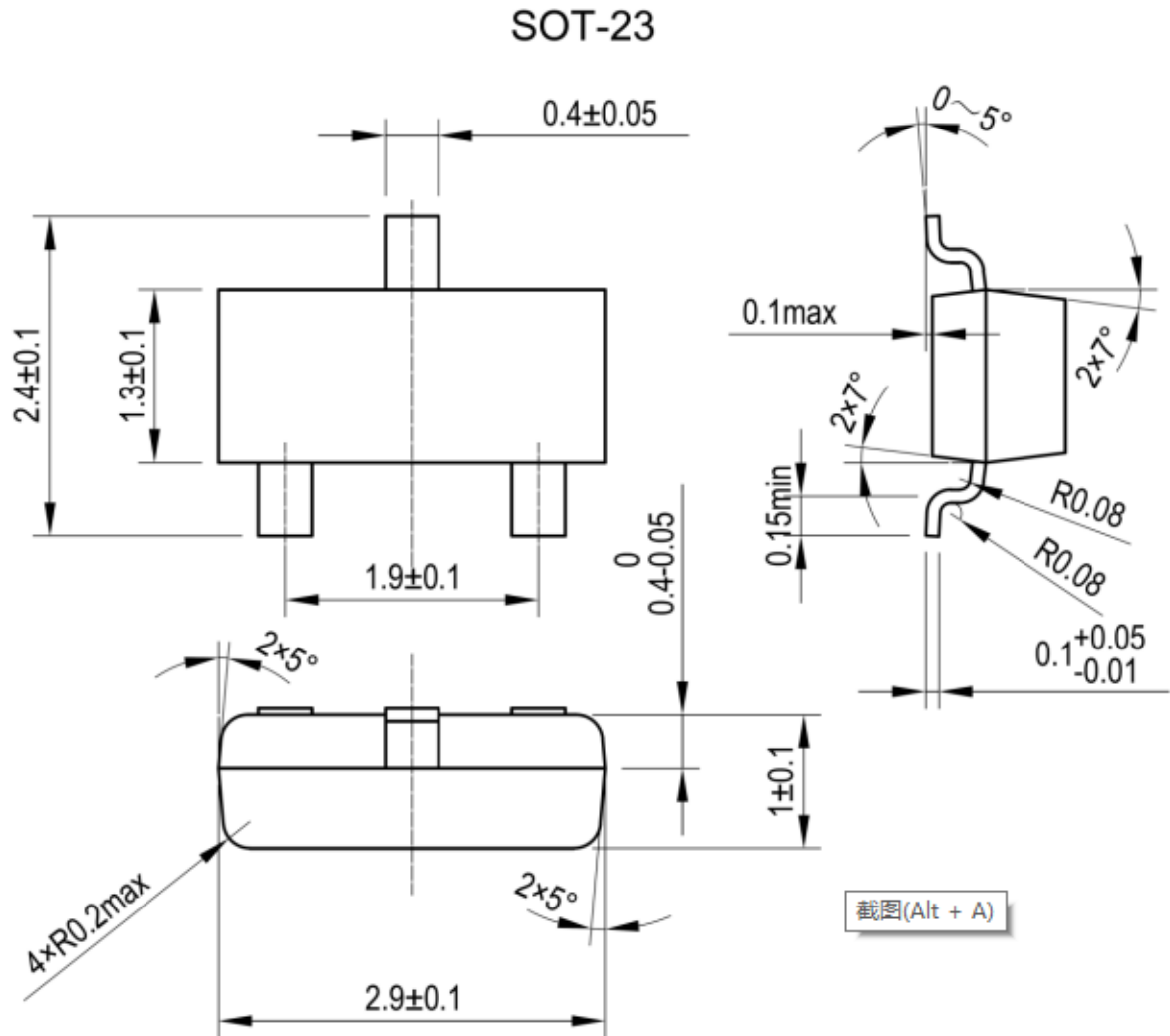


Fig. 4.2 Unclamped Inductive Switching Waveforms



Package Outline Drawing





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