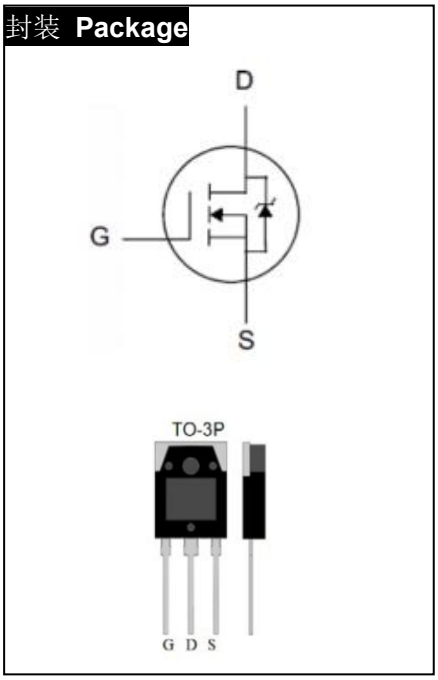
XTMF50N46P

500V N-ch Planar MOSFET

封装 **Package**



Product Description

BV_{DSS}	500	V
I_D	46	A
$R_{DS(ON),Typ.}$	85	mΩ

General Features

- Advanced Planar Process
- $R_{DS(ON),typ.}$=85mΩ@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Rugged Poly silicon Gate Structure

Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

Device	Package	Marking
XTMF50N46P	TO-3P	XTMF50N46P

Absolute Maximum Ratings T_j=25℃

Symbol	Parameter	XTMF50N46P	Unit
V_{DSS}	Drain-to-Source Voltage	900	V
V_{GSS}	Gate-to-Source Voltage	±30	
I_D	Continuous Drain Current	46	A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	180	
E_{AS}	Single Pulse Avalanche Energy	5000	mJ
P_D	Power Dissipation	540	W
	Derating Factor above 25℃	4.32	W/℃
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	XTMF50N46P	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.23	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	℃/W

Electrical Characteristics T_j=25℃

OFF Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
BV_{DSS}	Drain-to-Source Breakdown Voltage	500	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	5	uA	V_{DS}=500V, V_{GS}=0V
		--	--	500		V_{DS}=400V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance[4]	--	85	100	mΩ	V_{GS}=10V, I_D=23A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance[4]	--	32	--	S	V_{DS} =25V, I_D=23A

Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
C_{iss}	Input Capacitance	--	6.8	--	nF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	0.1	--		
C_{oss}	Output Capacitance	--	0.7	--		
Q_g	Total Gate Charge	--	138	--	nC	V_{DD}=250V, I_D=23A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	38	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	27	--		

Resistive Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$t_{d(ON)}$	Turn-on Delay Time	--	25	--	ns	V_{DD}=250V, I_D=23A, V_{GS}= 10V R_G=10Ω
t_{rise}	Rise Time	--	39	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	100	--		
t_{fall}	Fall Time	--	36	--		

Source-Drain Body Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{SD}	Continuous Source Current[4]	--	--	46	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[4]	--	--	180		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=46A, V_{GS}=0V
trr	Reverse recovery time	--	730	--	ns	V_{GS}=0V ,I_F=46A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	3.0	--	uC	

[1] Pulse width≤380μs; duty cycle≤2%

Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

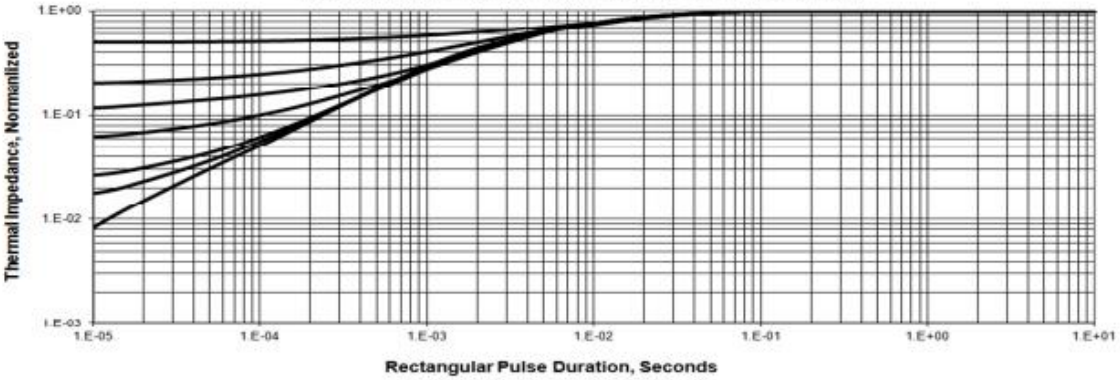


Figure 2 . Max. Power Dissipation vs Case Temperature

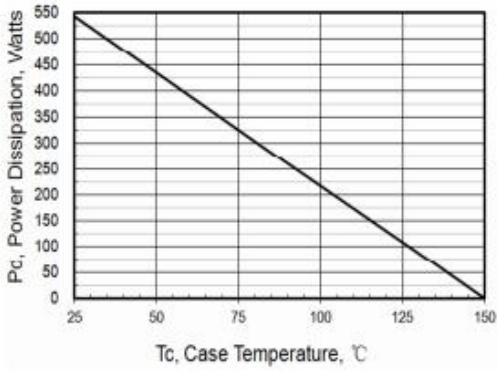


Figure 3 .Maximum Continuous Drain Current vs Tc

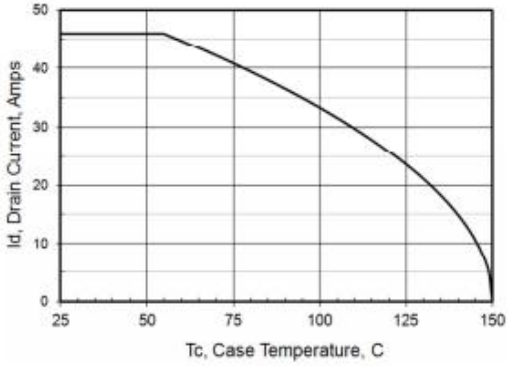


Figure 4. Typical Output Characteristics

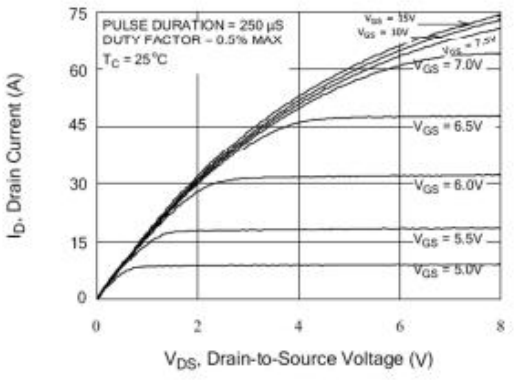
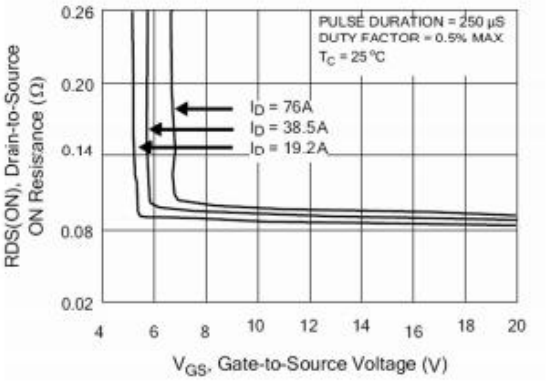


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current



Typical Characteristics(Cont.)

Figure 6. Peak Current Capability

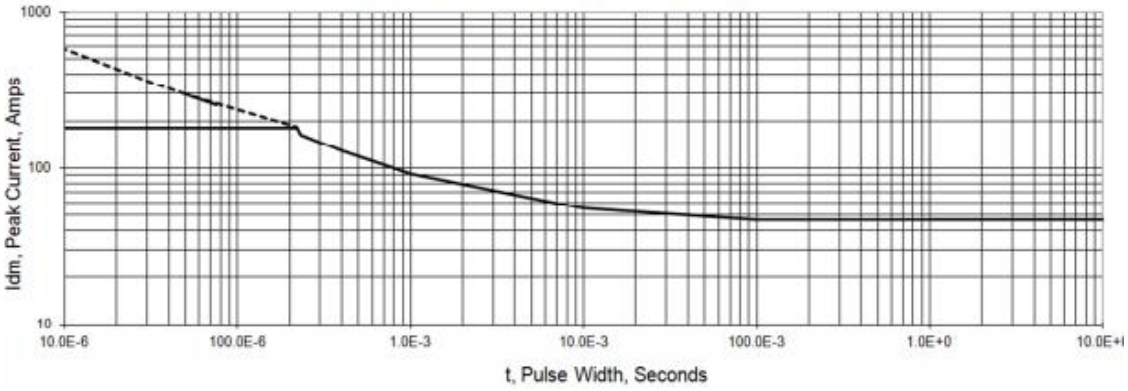


Figure 7. Typical Transfer Characteristics

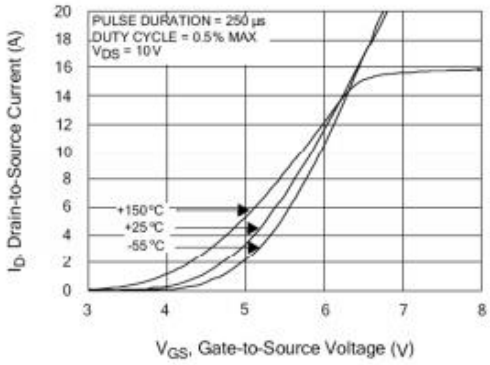


Figure8. Unclamped Inductive Switching Capability

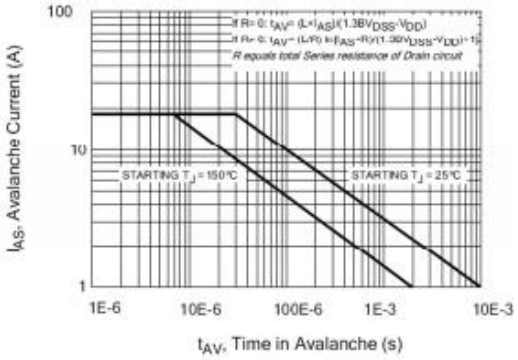


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

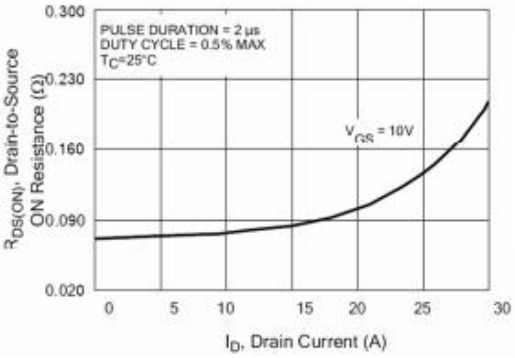
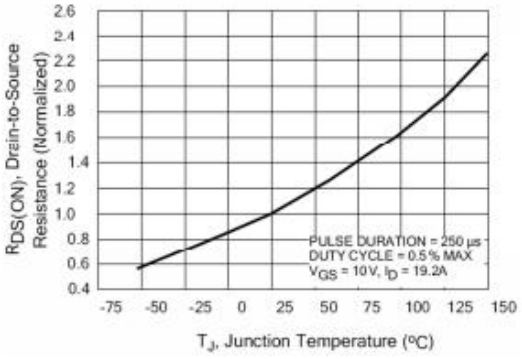


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature



Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs Junction Temperature

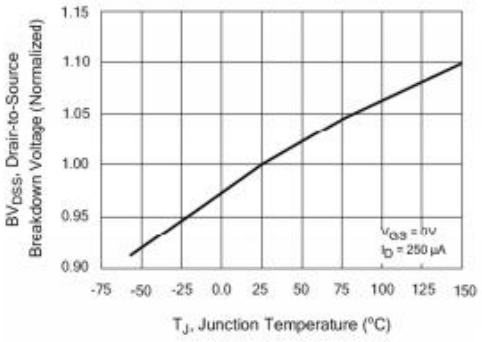


Figure 12. Typical Threshold Voltage vs Junction Temperature

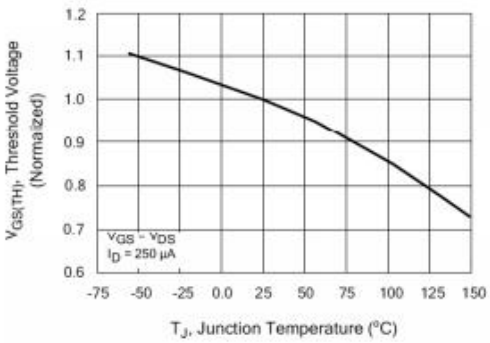


Figure 13. Maximum Forward Bias Safe Operating Area

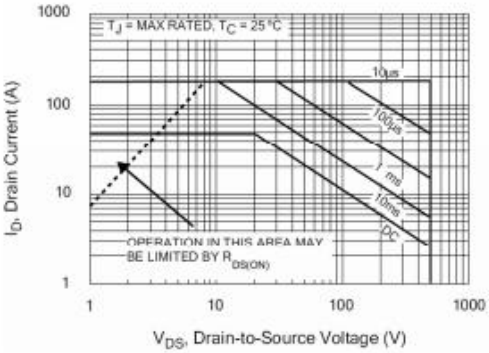


Figure 14. Typical Capacitance vs Drain-to-Source Voltage

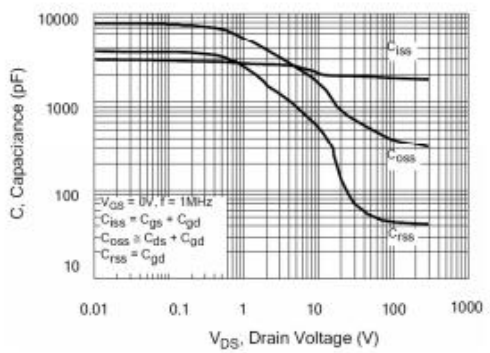


Figure 15. Typical Gate Charge vs Gate-to-Source Voltage

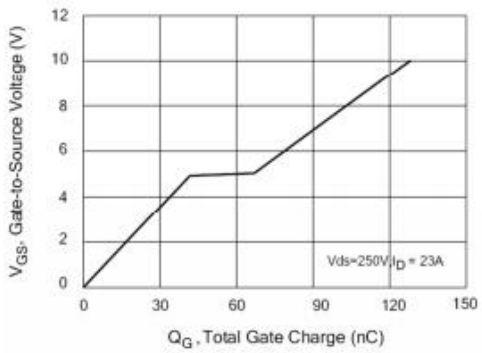
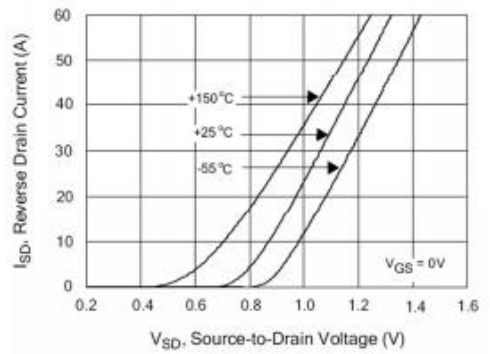


Figure 16. Typical Body Diode Transfer Characteristics



Test Circuits and Waveforms

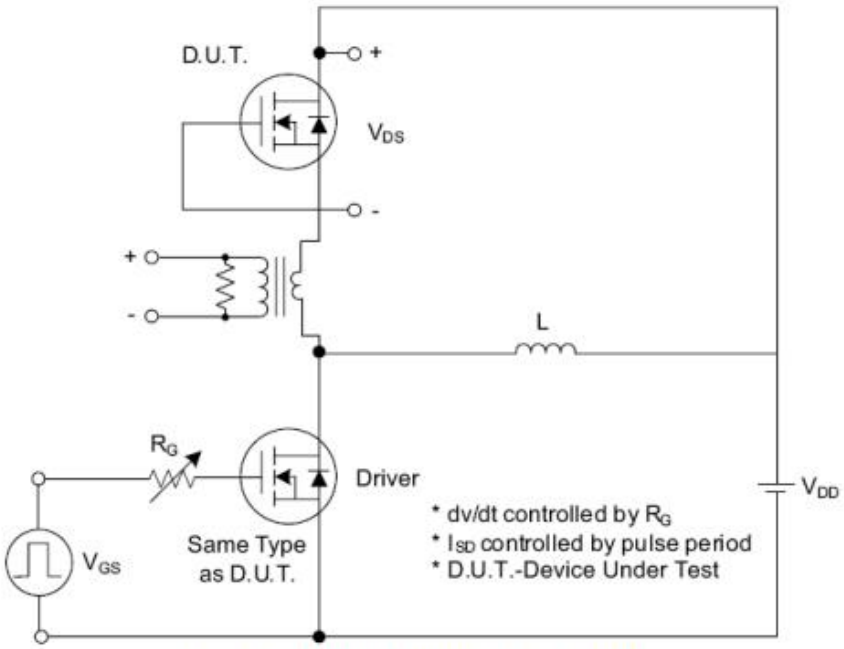


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

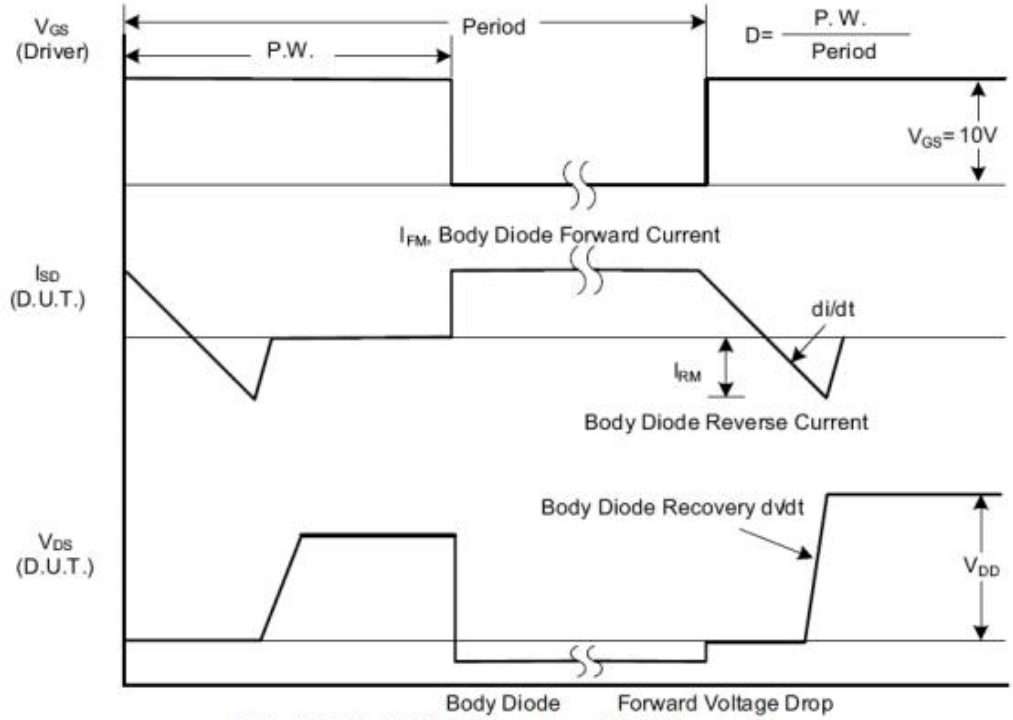


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

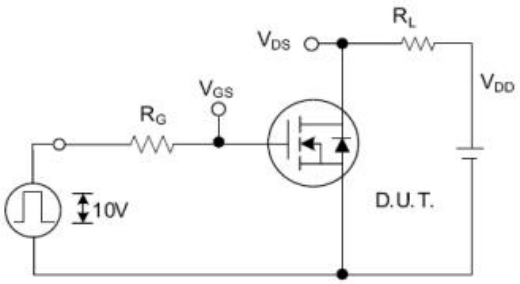


Fig. 2.1 Switching Test Circuit

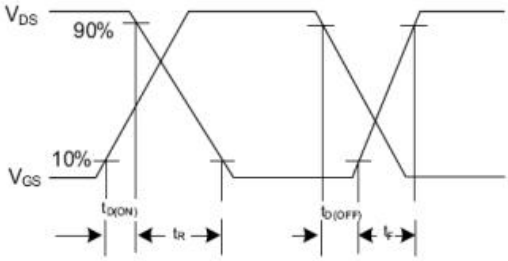


Fig. 2.2 Switching Waveforms

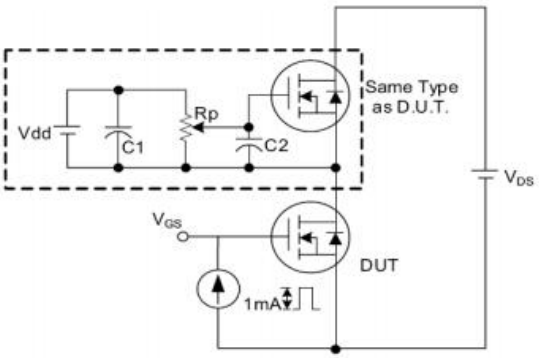


Fig. 3 . 1 Gate Charge Test Circuit

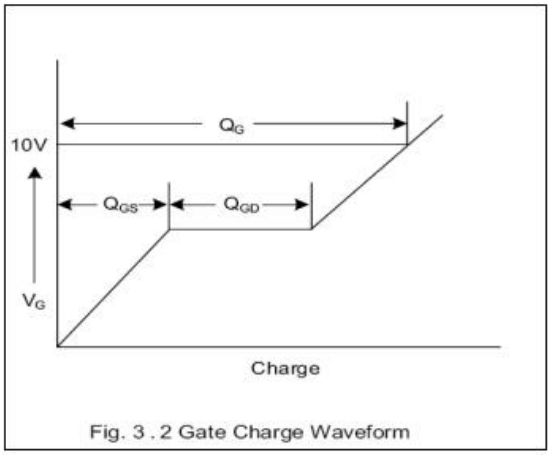


Fig. 3 . 2 Gate Charge Waveform

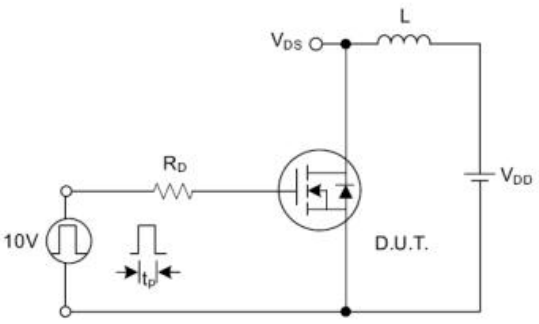


Fig. 4.1 Unclamped Inductive Switching Test Circuit

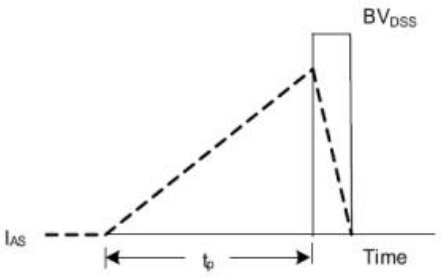


Fig. 4.2 Unclamped Inductive Switching Waveforms