XTMF90N09P

900V N-ch Planar MOSFET

Product Description
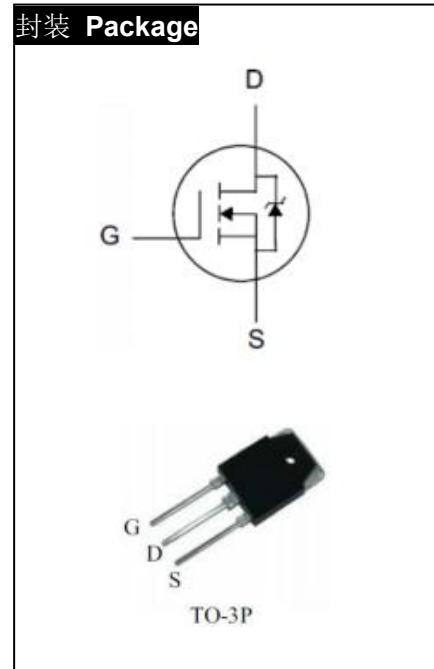
| BV$_{DSS}$	900	V
I$_D$	9	A
R$_{DS(ON),Typ.}$	1.1	Ω

General Features

- Proprietary New Planar Technology
- R$_{DS(ON),typ.}$=1.1Ω@V$_{GS}$=10V
- Fast Recovery Body Diode
- Low Gate Charge Minimize Switching Loss

Applications

- Adaptor Charger
- SMPS Power Supply
- LCD Panel Power

封装 **Package**

TO-3P

Device	Package	Marking
XTMF90N09P	TO-3P	XTMF90N09P

Absolute Maximum Ratings   T$_j$=25℃

Symbol	Parameter	XTMF90N09P	Unit
V$_{DSS}$	Drain-to-Source Voltage	900	V
V$_{GSS}$	Gate-to-Source Voltage	±30	
I$_D$	Continuous Drain Current	9	A
I$_{DM}$	Pulsed Drain Current at V$_{GS}$=10V	36	
E$_{AS}$	Single Pulse Avalanche Energy	850	mJ
P$_D$	Power Dissipation	250	W
	Derating Factor above 25℃	2.0	W/℃
T$_L$	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	℃
T$_J$& T$_{STG}$	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	XTMF90N09P	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.50	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	℃/W

Electrical Characteristics T_j=25℃

OFF Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
BV_{DSS}	Drain-to-Source Breakdown Voltage	900	-	-	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	-	-	1	uA	V_{DS}=900V, V_{GS}=0V
		-	-	250		V_{DS}=720V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	-	-	+100	nA	V_{GS}=+30V, V_{DS}=0V
		-	-	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance[4]	--	1.1	1.4	Ω	V_{GS}=10V, I_D=4.5A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance[4]	--	11	--	S	VDS=30V,ID=9A
Rg	Gate Resistance	--	1.0	--	Ω	Vds=0V,F=1MHz

Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
C_{iss}	Input Capacitance	--	2200	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	50	--		
C_{oss}	Output Capacitance	--	180	--		
Q_g	Total Gate Charge	--	70	--	nC	V_{DD}=450V, I_D=9A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	9.0	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	32	--		

Resistive Switching Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$t_{d(ON)}$	Turn-on Delay Time	--	40	--	ns	V_{DD}=450V, I_D=9A, V_{GS}= 10V R_G=4.7 Ω
t_{rise}	Rise Time	--	44	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	120	--		
t_{fall}	Fall Time	--	50	--		

Source-Drain Body Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_{SD}	Continuous Source Current[4]	--	--	9	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[4]	--	--	36		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=9A, V_{GS}=0V
trr	Reverse recovery time	--	680	--	ns	V_{GS}=0V ,I_F=9A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	5.0	--	uC	

[1] Pulse width≤380μs; duty cycle≤2%

Typical Characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case
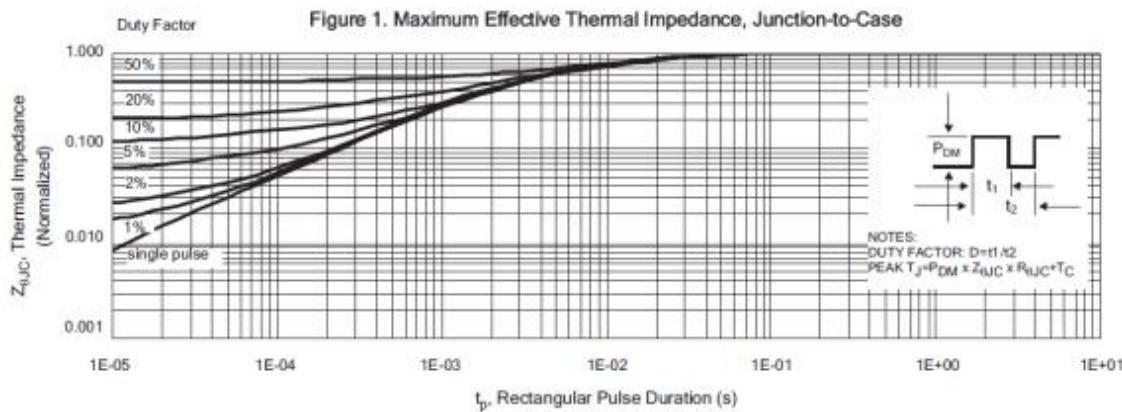
Figure 2 . Maximum Power Dissipation vs Case Temperature

Figure 3 .Maximum Continuous Drain Current vs Case Temperature

Figure 4. Typical Output Characteristics
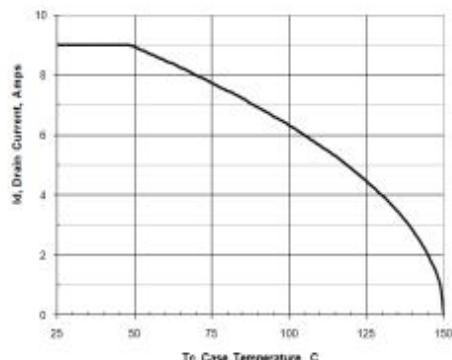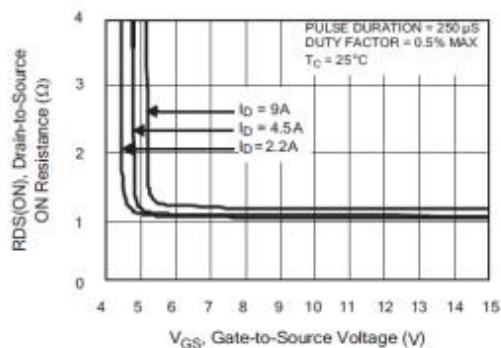
Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

Typical Characteristics(Cont.)

Figure 6. Maximum Peak Current Capability
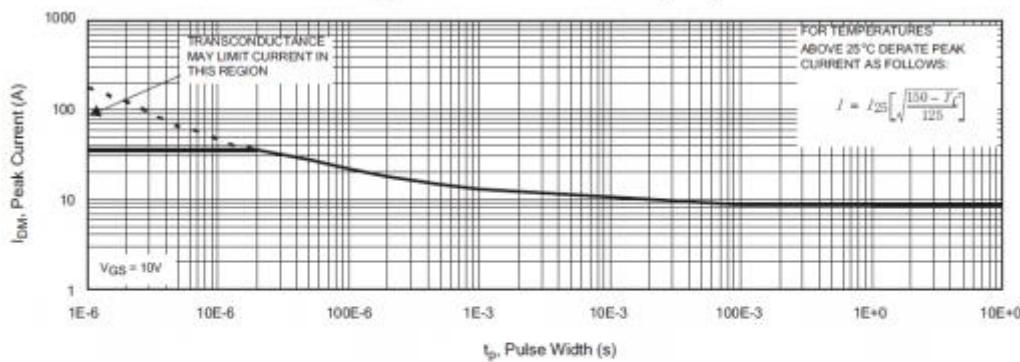

Figure 7. Typical Transfer Characteristics

Figure8. Unclamped Inductive Switching Capability
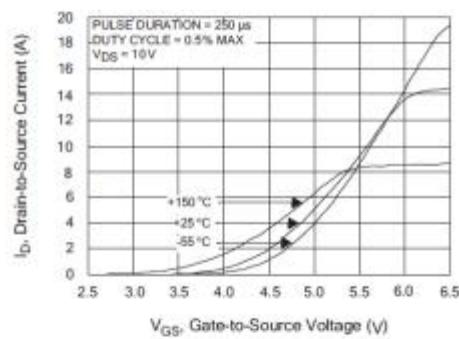
Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current
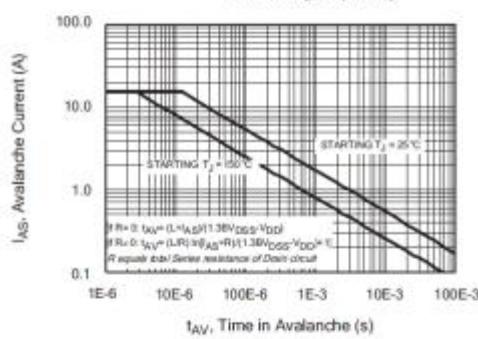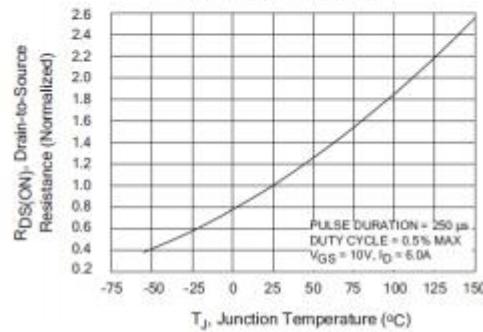
Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

Typical Characteristics(Cont.)

Figure 11. Typical Breakdown Voltage vs Junction Temperature

Figure 12. Typical Threshold Voltage vs Junction Temperature

Figure 13. Maximum Forward Bias Safe Operating Area
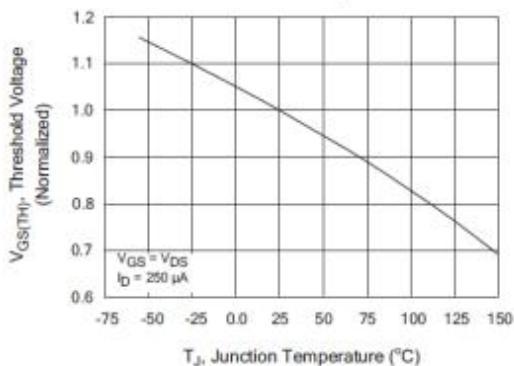
Figure 14. Capacitance vs Vds

Figure 15 . Typical Gate Charge
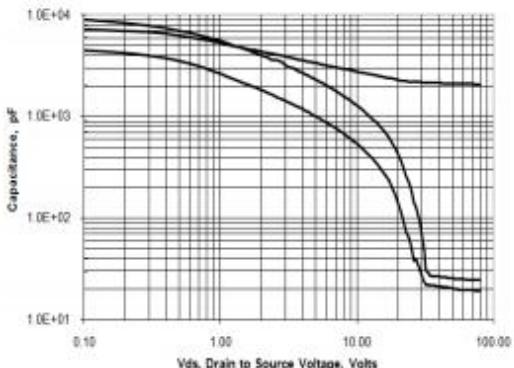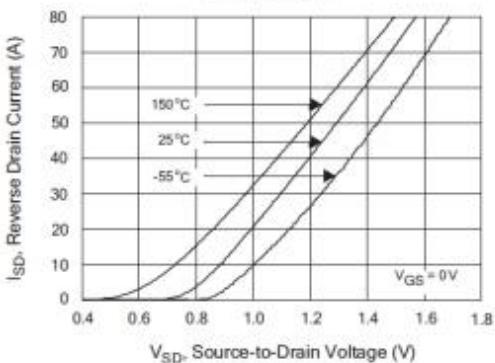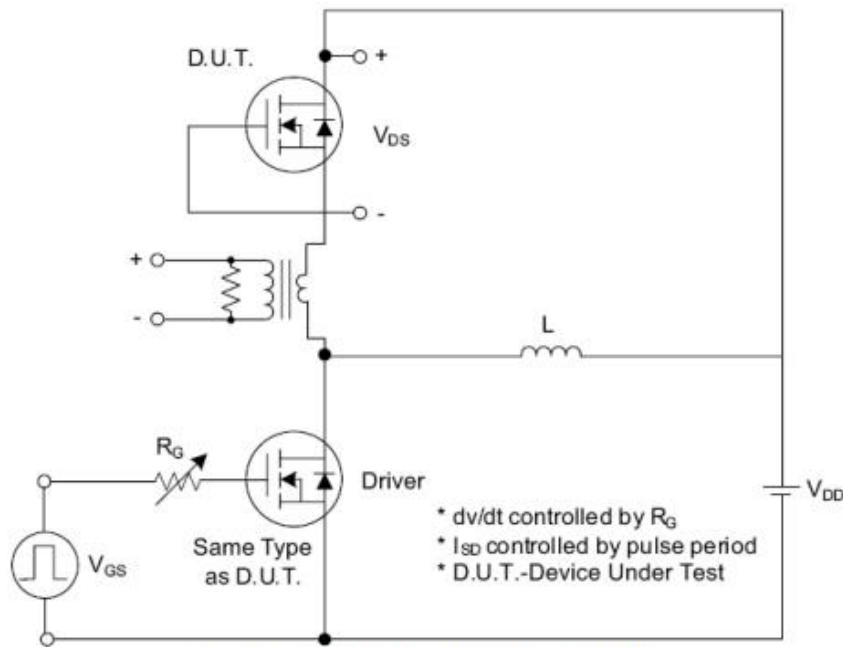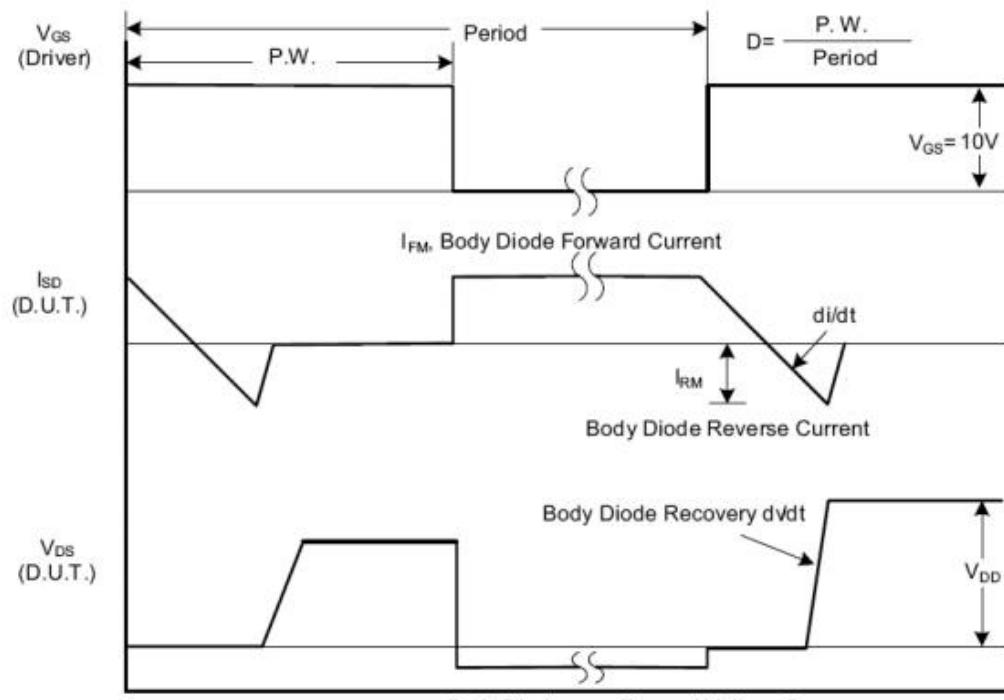
Figure 16. Typical Body Diode Transfer Characteristics

Test Circuits and Waveforms


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

* dv/dt controlled by R_G
* I_{SD} controlled by pulse period
* D.U.T.-Device Under Test

Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)
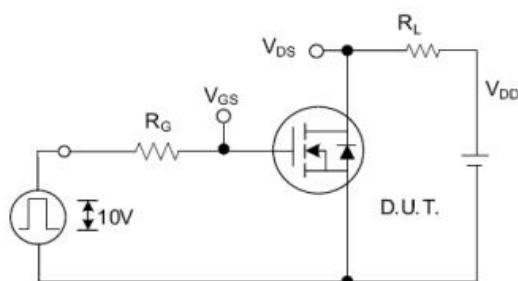

Fig. 2.1 Switching Test Circuit
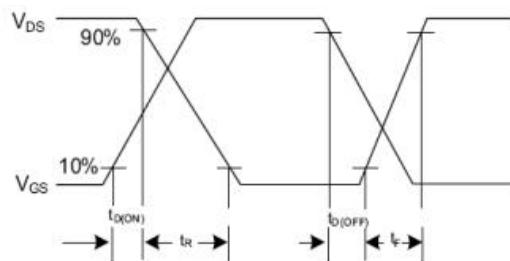

Fig. 2.2 Switching Waveforms
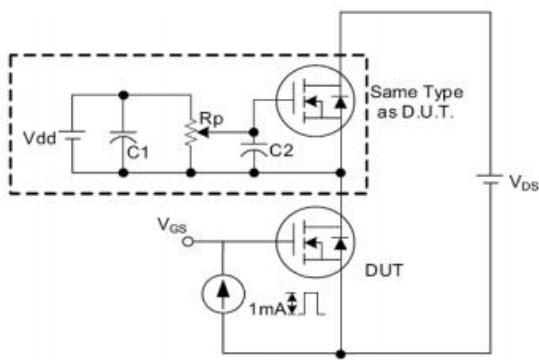
Fig. 3 . 1 Gate Charge Test Circuit
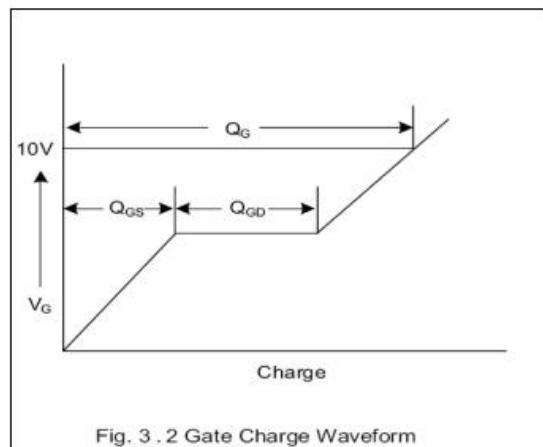
Fig. 3 . 2 Gate Charge Waveform
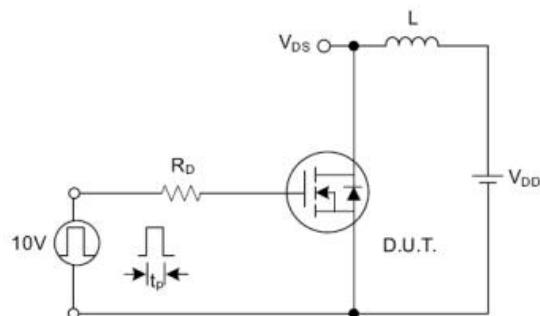

Fig. 4.1 Unclamped Inductive Switching Test Circuit
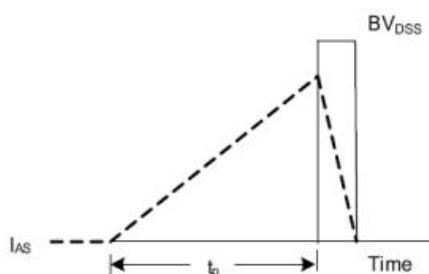
Fig. 4.2 Unclamped Inductive Switching Waveforms